S- AND KU-BAND FREQUENCY SOURCE DEVELOPMENT

FINAL REPORT

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1. INTRODUCTION AND SUMMARY

This final report describes the results of the two part S- and Ku-band source development program. The S- and Ku-band sources were designed, fabricated, and evaluated under NASA contracts NAS5-23822 and NAS5-25354. The primary purpose of this effort was to demonstrate a high performance S- and Ku-band microwave signal source using state-of-the-art SAW oscillator and microwave source technology. The first part of this program had four primary objectives:

- Design and fabricate two 2.14 GHz SAW delay line oscillators
- Fabricate 2.14 GHz $A\ell N/A\ell_2O_3$ delay lines for the oscillators
- Fabricate and evaluate two wafer runs of 2.14 GHz TED devices
- Fabricate a 15 GHz frequency source using the 2.14 GHz SAW oscillator as a frequency reference.

The second part of this development program extended the technology started on the initial contract. The specific areas addressed during the second S- and Ku-band source contract were to:

- Investigate the t/λ ratio $A\ell N/A\ell_2O_3$ delay line frequency adjustment range
- Fabricate two S-band $A\ell N/A\ell_2O_3$ delay lines
- Design and fabricate a 2.14 GHz hybrid packaged SAW oscillator
- Design and fabricate a temperature stable TED divider circuit
- Fabricate a Ku-band frequency source using a TED frequency divider.

The report addresses each of the various program tasks on a topical basis; i.e., the SAW oscillator work performed during both contracts is discussed in one section.

A key element in the fabrication of the S- and Ku-band sources is the 2.14 GHz $A\ell N/A\ell_2O_3$ high velocity delay lines used as the frequency determining element in the SAW reference oscillators. Section 2 of this report describes the design, fabrication, and theory of operation of the $A\ell N/A\ell_2O_3$ delay lines in detail. This section also describes the use of the t/λ frequency characteristic of the $A\ell N/A\ell_2O_3$ substrates as a delay line frequency adjusting mechanism.

The 2.14 GHz SAW oscillators fabricated for this program are described in Section 3 of this report. Two oscillator designs were fabricated during the course of the two contracts. The first 2.14 GHz oscillator was built using discrete components and commercially available RF hybrid circuits. This unit included an active temperature compensating circuit. The second 2.14 GHz SAW oscillator was a hybrid packaged version of the discrete component unit.

The TRW-developed TED divider work is described in Section 4. During the initial phase of this effort, several wafer runs of 2.14 GHz TED's were fabricated and evaluated as a 15 GHz divider. The TED 15 GHz divide-by-seven circuit was optimized and used as the frequency divider element in the 15 GHz phaselocked frequency source.

The complete Ku-band sources are described in Section 5. Two types of sources were constructed and evaluated. During the first contract a multiplier type phaselocked 15 GHz source was fabricated and tested. The multiplier source multiplies the 2.14 GHz reference signal to 15 GHz. The 15 GHz reference signal is used to phaselock the 15 GHz VCO. A divider type 15 GHz source was built during the second contract. The divider source uses a TED divide-by-seven to divide the 15 GHz VCO output to 2.14 GHz for phase comparison with the reference signal. The performance of the two 15 GHz signal sources was compared on the basis of performance, size, weight, and power.

2. AℓN/$Aℓ_2O_3$ DELAY LINE STUDY

Aluminum nitride (AℓN) is an attractive substrate for surface acoustic wave (SAW) applications due to its piezoelectricity and high SAW velocity. The high velocity is particularly useful for devices operating above 2 GHz. At these frequencies, the photolithographic requirements are extremely stringent. By using a high velocity substrate, the stringent resolution can be relaxed, resulting in higher device yield and better device performance.

Unfortunately, aluminum nitride has not been available in single bulk crystal form. To obtain useful SAW substrates, a thin AℓN film is grown epitaxially on sapphire ($Aℓ_2O_3$). The use of sapphire is attractive for the following reasons. First, the SAW velocity on sapphire is high and is comparable with that of AℓN. Second, the lattice dimension of sapphire at certain crystal planes matches well with that of the AℓN, resulting in good epitaxial growth. For these reasons, AℓN/$Aℓ_2O_3$ has been chosen as the substrate for the 2 GHz SAW delay line.

2.1 OBJECTIVE

The overall objectives of the study were to demonstrate the use of a new, high velocity SAW substrate material (AℓN/$Aℓ_2O_3$) for delay lines operating at above 2 GHz and to develop an economical procedure for setting the operating frequency of SAW delay lines on AℓN/$Aℓ_2O_3$ during device fabrication. To accomplish these goals, the following tasks were undertaken:

- Growth and characterization of AℓN/$Aℓ_2O_3$.
- 2.2 GHz SAW delay line, fabrication and packaging.
- Theoretical and experimental investigation of SAW velocity dispersion and temperature coefficient in AℓN/$Aℓ_2O_3$.
- Fabrication of delay lines to meet NASA/TRW frequency requirements.

The following sections will discuss each of these four tasks in greater detail.

2.2 GROWTH AND CHARACTERIZATION OF $A\ell N/A\ell_2O_3$

2.2.1 Vapor Phase Epitaxial Growth of $A\ell N$ on $A\ell_2O_3$

$A\ell N/A\ell_2O_3$ substrates are not commercially available. As a result, TRW grew all materials required for the program. The growth technique adopted was the vapor phase epitaxial (VPE) growth technique which was described in the literature[1,2,3,4] and reportedly produced the best $A\ell N/A\ell_2O_3$ material for SAW applications.

The schematic of the vapor phase epitaxial (VPE) reactor is shown in Figure 2-1. The $A\ell N$ film is grown by chemical reaction between a metal-organic gas, $(CH_3)_3A\ell$, trimethylaluminum (TMA) and ammonia. Hydrogen was used as the carrier gas. The flow rates for the different gases were: 8 ℓ/min direct hycrogen, 0.8 ℓ/min ammonia, and 30 cc/min H_2 bubbled through TMA plus 1ℓ/min ammonia, and 30 cc/min H_2 bubbled through TMA plus 1 ℓ/min backup flow. The sapphire substrate was placed on a rotating susceptor made of graphite. This susceptor was RF heated to 1200°C during growth. The temperature was monitored by an optical pyrometer. The $A\ell N$ films were grown at a rate of approximately 1.5 μm/hour.

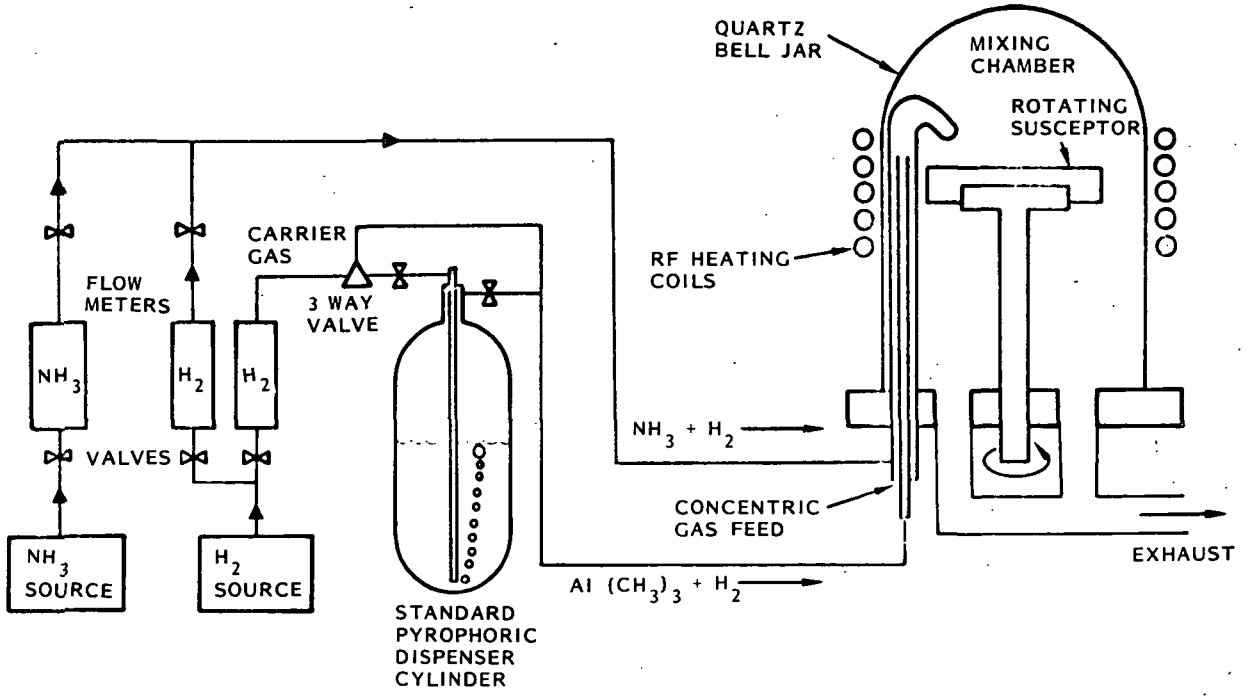

Figure 2-1. Vapor Epitaxial Reactor

Prior to growth, the sapphire substrates were hydrogen-etched while substrates were being brought up to growth temperature. The AℓN films were usually grown for two hours to a thickness of about 3 μm. During growth, the susceptor was slowly rotated at 6 rpm to ensure uniform growth. After growth, the susceptor was slowly cooled over a period of two hours to room temperature. The AℓN films were grown on the R-plane of sapphire. The epitaxial relationship of AℓN to sapphire has been previously reported.[5] The c-axis direction of AℓN on the R-plane of sapphire has been found to possess a high electromechanical coupling coefficient.[1,2,3]

2.2.2 Film Characterization by Scanning Electron Microscopy

The quality of the $A\ell N/A\ell_2O_3$ was first evaluated by using a scanning electron microscope (SEM). The surface morphology was found to correlate with the piezoelectric properties of the film. For good films, the axis of all small single crystals will line up. Figure 2-2 shows an example of a good film on R-plane sapphire. The AℓN film was grown coherently. The magnification for this photo is 5000X and the typical grain size is 1.0 μm. This high quality film processes a high electromechanical coupling coefficient.

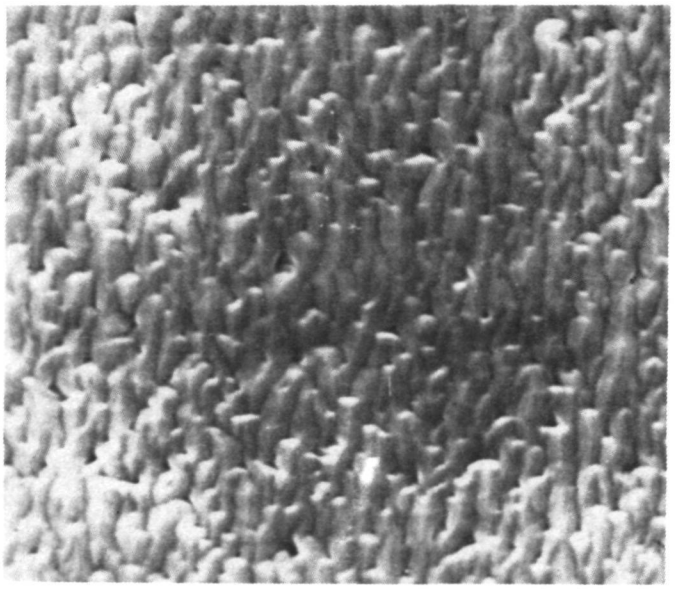

Figure 2-2. Surface Morphology of AℓN on R-Plane Sapphire

2.3 2.2 GHz SAW DELAY LINE DESIGN, FABRICATION, AND PACKAGING

2.3.1 2.2 GHz SAW Delay Line Design

The SAW delay line is the frequency controlling element of the SAW oscillator. The important parameters for the delay line are the time delay (τ), 3 dB bandwidth and insertion loss. The time delay determines the mode spacing as well as the effective Q of the oscillator. The mode spacing is given as $1/\tau$, while the effective Q is $\omega\tau/2$, ω is the operating frequency in radians. For SAW oscillators, the 3 dB bandwidth of the delay line must be smaller than the mode spacing so only a single mode can oscillate. The insertion loss is also important in the design because the amplifier gain must exceed the insertion loss for the oscillator to oscillate. Furthermore, lower insertion loss results in a lower noise floor for the oscillator.

Taking all these matters into consideration, the delay line shown schematically in Figure 2-3 was designed. The delay line consists of two transducers, each with the thinned electrode configuration. This thinned electrode design is a modification of the conventional interdigital transducer design in that sections of fingers are removed from the conventional transducer.

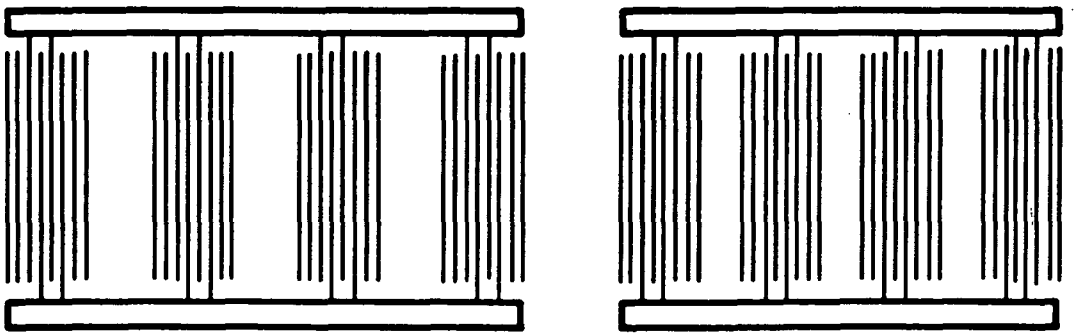

Figure 2-3. Thinned Electrode Transducer Design

The advantage of removing these fingers is that the propagation loss due to the presence of an excessive number of metal fingers on the substrate surface is minimized while the total length of the transducer is preserved, keeping the desired narrow bandwidth required for single mode operation. The thinned electrode design, on the other hand, produces a secondary passband whose frequency is determined by the section-to-section

separation. By designing different section-to-section separations for the input and output transducers, the secondary passband will occur at different frequencies for these transducers. As a result, only one passband remains for the delay line.

Table 2-1 summarizes the design parameters for the 2 GHz SAW delay line. The computer simulated frequency response using the delta function model is shown in Figure 2-4. This delay line will result in an effective Q of 1570 for the oscillator.

Table 2-1. Delay Line Design Summary

	Transducer A	Transducer B
Number of Sections	20	20
Finger Pairs/Section	5	5
Section Separation (λo)	15	25
*Aperture Width = 57 λo		
*Center-to-Center Separation = 500 λo		
*Fingerwidth = 0.66 μm		

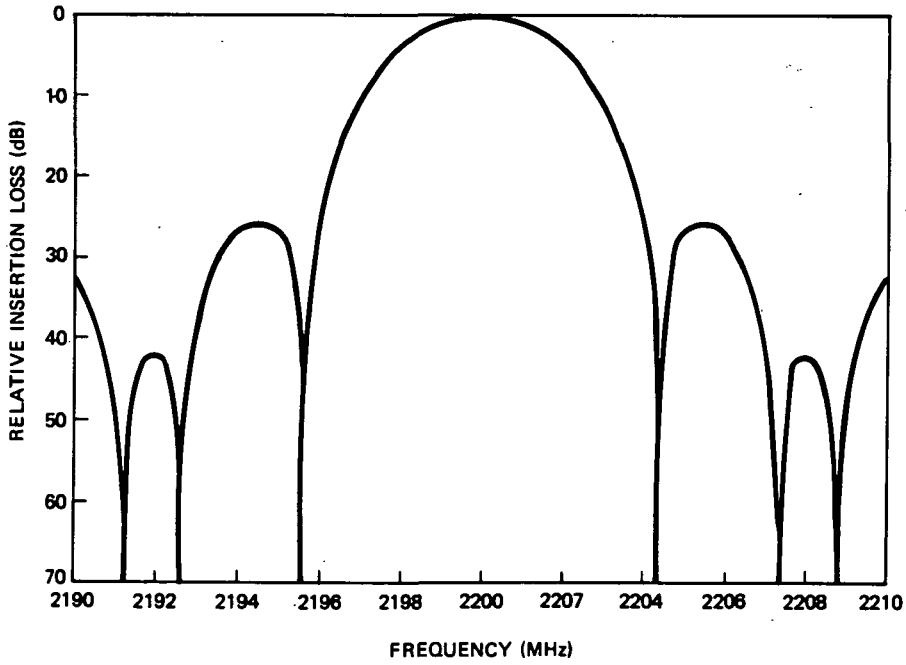

Figure 2-4. Computer Simulated Frequency Response of the 2.2 GHz SAW Delay Line on $A\ell N/A\ell_2O_3$

2.3.2 2 GHz Delay Line Fabrication

The 2 GHz delay line was fabricated by using the conventional photolithographic technique. The critical steps in the device fabrication are photomask generation, substrate polishing, and contact printing. The following paragraphs describe the technique through which all these steps are accomplished.

Photomask Generation

The photomask with submicron linewidths was fabricated at TRW using an Applicon system, Electromask pattern generator, and an Electromask step-and-repeat machine. All the dimensions of the transducer pattern are read into the Applicon system and stored before transfer to the HP2100 computer which controls the 2000 Electromask pattern generator which, in turn, generates the 10X reticle. The pattern generator consists of a xenon light, a variable aperture assembly, an XY stage, and a 10X reduction camera. When both the size of the aperture and the position of the XY stage match the data in the computer, the xenon lamp is flashed and the image is made. The positional accuracy of the XY stage is monitored by a helium-neon laser interferometer system. Position precision is ±10 microinches over a 5 x 5 inch area. To complete the mask fabrication, the reticle was put into a step-and-repeat camera system (1000 Electromask Image Repeater) to make the final reduction.

Substrate Polishing

Figure 2-2 displays the surface of a typical AℓN film grown epitaxially on $Aℓ_2O_3$ by VPE, which is very rough. To fabricate the device, the surface must be polished. Furthermore, as will be discussed in later sections, the thickness of the AℓN film has a direct effect on the device performance. It is therefore necessary to precisely control the thickness of the AℓN film.

The AℓN/$Aℓ_2O_3$ was mechanically polished using Monsanto Syton polish as the polishing agent. The thickness of the AℓN film is monitored by cutting grooves into the AℓN film and then counting the optical interference fringes of a monochromatic sodium light at the groove edges. This method provides a rough indication of the film thickness to an order of several thousand angstroms.

Contact Printing

The fabrication procedure of the delay line is shown schematically in Figure 2-5. In this lift-off technique, a dark field flexible mask was used to expose the Shipley 1350J photoresist which was coated onto the $A\ell N/A\ell_2O_3$ substrate. After developing the exposed photoresist, aluminum metal is evaporated onto the relief pattern. The crucial step in this process is the ability to define submicron lines during the exposure. This is because the device linewidth is not much larger than the wavelength of the exposure light, and if the mask is not in close contact with the substrate, the light diffraction would smear the line definition.

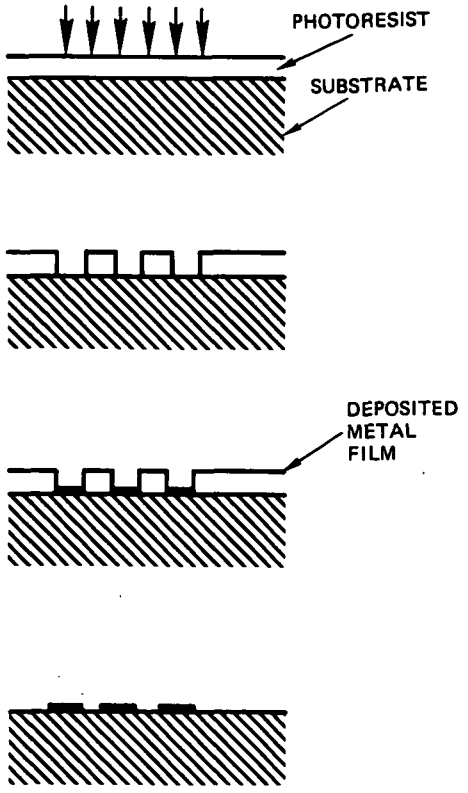

Figure 2-5. Lift-Off Technique Delay Line Processing Steps

To achieve maximum linewidth resolution, a conformal vacuum frame using a thin rubber membrane to lift the $A\ell N/A\ell_2O_3$ substrate into intimate contact with the flexible photomask was used. A conformal vacuum frame holder was built using the guidelines developed at MIT Lincoln Laboratory. Figure 2-6 shows the various parts of the conformal vacuum frame holder, and Figure 2-7 shows it assembled and in operation. For the UV exposure,

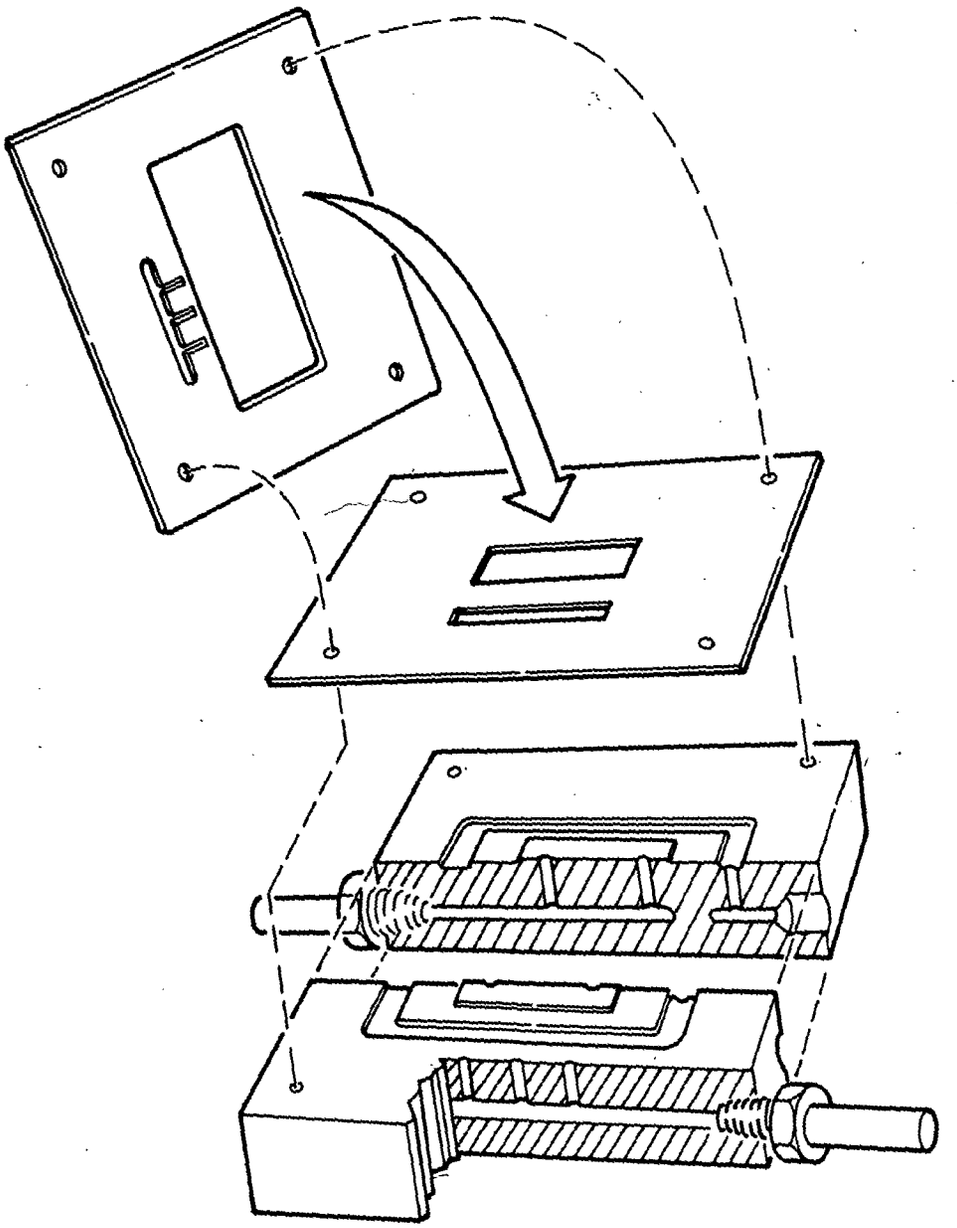

Figure 2-6. Comfortable Vacuum Frame

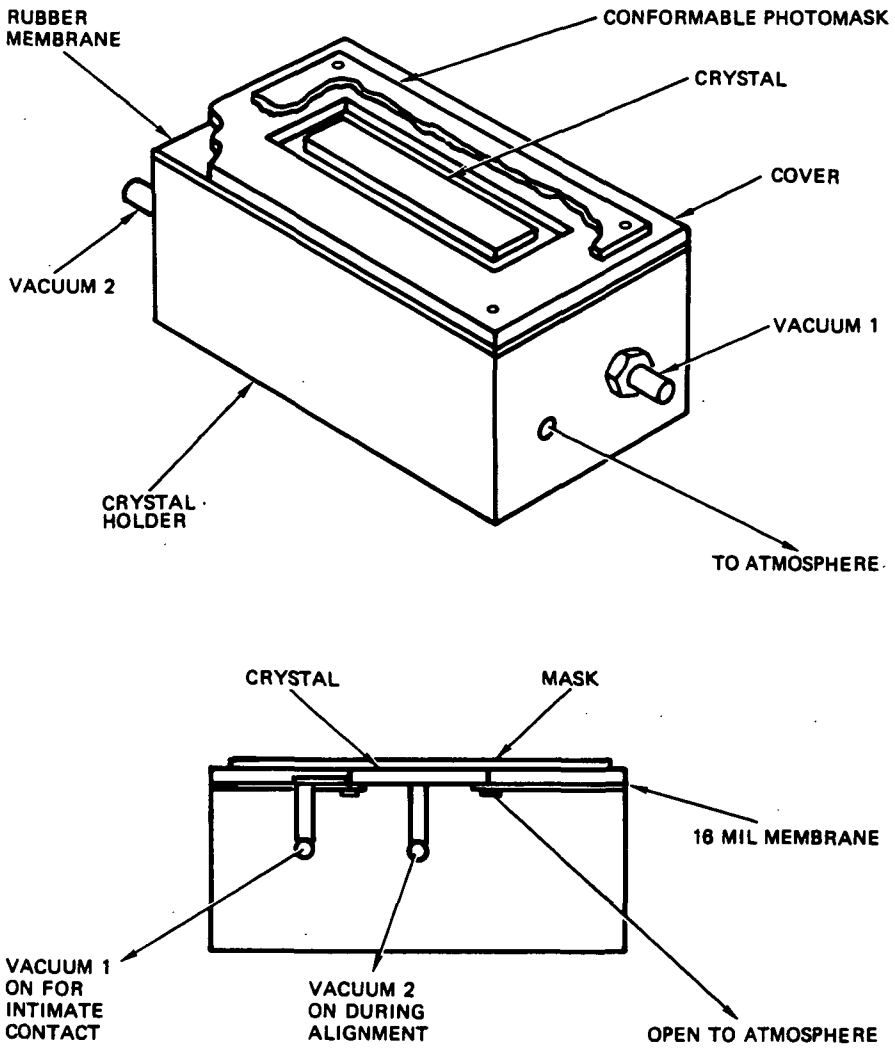

Figure 2-7. Vacuum Frame Operational Details

the following sequence of steps is followed. First, the crystal or substrate is held down during alignment by evacuating port 1. The flexible photomask is pulled into intimate contact with the crystal by evacuating port 2, and is bowed as it makes intimate contact. To eliminate this bowing, the vacuum in port 1 is released to atmospheric pressure. In doing so, the rubber membrane lifts the crystal upward, maintaining intimate contact while eliminating the bowing. The holder is then exposed to UV light which is highly collimated and of uniform exposure illumination.

2.3.3 2 GHz Delay Line Packaging

The 2 GHz delay is packaged in a standard flatpack as shown in Figure 2-8. The SAW crystal is mounted using an RTV adhesive which serves to isolate the SAW crystal from mechanical stresses. Connections from the delay line to the package are made using aluminum bond wires which also provide inductive matching between the capacitive transducers and 50Ω. The electrical isolation for this package is greater than 50 dB up to 3 GHz. The SAW delay line is hermetically sealed prior to the installation in an oscillator.

2.4 CHARACTERIZATION OF DELAY LINES ON AℓN/$Aℓ_2O_3$ — SAW VELOCITY DISPERSION AND TEMPERATURE COEFFICIENT

A variety of SAW delay lines were fabricated on the AℓN/$Aℓ_2O_3$ and their electrical response measured as a function of frequency as well as temperature variation. By doing so, one evaluates the basic material properties of the AℓN/$Aℓ_2O_3$ substrate and from these data optimizes the fabrication parameters in order to obtain delay lines which meet NASA/TRW requirements. The typical thickness of the AℓN film in these experiments is about 2 microns.

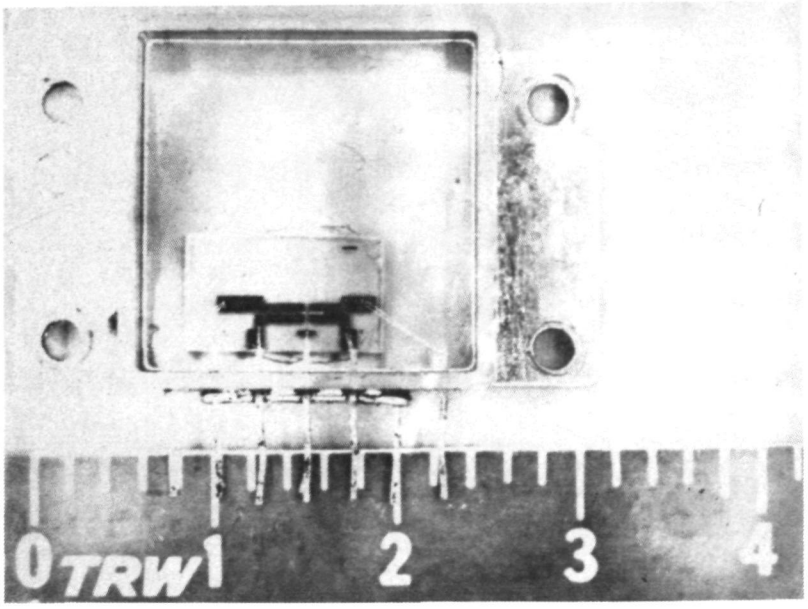

Figure 2-8. 2.2 GHz SAW Delay Line

2.4.1 Electromechanical Coupling

The electromechanical coupling coefficient k^2 was obtained by measuring the transducer's radiation resistance R_a, static capacitance C_s, and resonance frequency f_o. The static capacitance C_s for $A\ell N/A\ell_2O_3$ is about $1 \cdot 10^{13}$ pF/mm-pair. The electromechanical coupling coefficient k^2 was calculated from the following relation

$$k^2 = \frac{\pi^2}{2} f_o C_s R_a$$

The results show that k^2 remains approximately equal to about 0.3 percent for $t/\lambda > 0.8$ (where t is the AℓN film thickness and λ is the acoustic wavelength).

2.4.2 SAW Velocity Dependence on T/λ Ratio

Aluminum nitride on sapphire is a composite structure; therefore, the surface acoustic wave velocity is dependent upon the thickness of the AℓN layer. Figure 2-9 shows the relationship between velocity and the AℓN thickness to wavelength ratio (t/λ). The open circles show the original data taken by Lakin, et al. The closed triangles are TRW's measurements. For t/λ ratios of 0.75 and less, the two sets of data agree reasonably well. For t/λs of 0.75, TRW's data shows a leveling off of velocity. The penetration depth of the surface acoustic wave into the substrate is about on wavelength. As the ratio t/λ increases, more and more of the surface acoustic wave is confined to the AℓN film. Thus, the leveling is due to the fact that SAW is confined mostly to the AℓN. It indicates the true property of the AℓN film.

2.4.3 Temperature Coefficient of Delay

The temperature coefficient of delay was determined by measuring the frequency change of the SAW delay line oscillator as a function of frequency. The results are shown in Figure 2-10, along with Liu's results. Earlier, it was speculated that AℓN had a negative temperature coefficient of delay. Because $A\ell_2O_3$ has a positive coefficient of delay, the $A\ell N/A\ell_2O_3$ structure was expected to have a zero first order coefficient of delay at

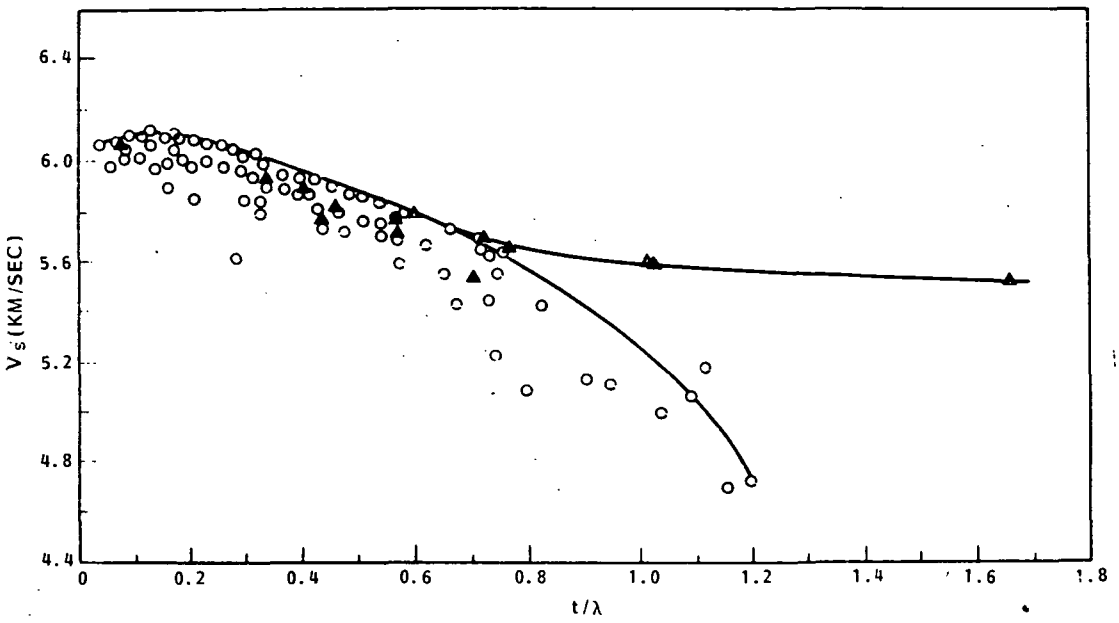

Figure 2-9. SAW Phase Velocity V_s Versus τ/λ, along AℓN C-Axis

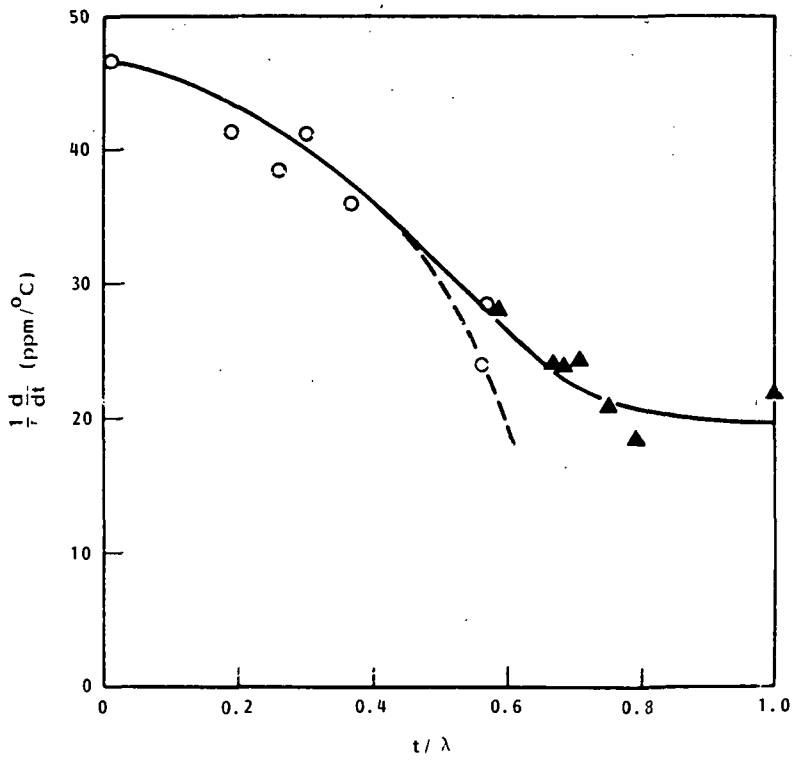

Figure 2-10. Temperature Coefficient of Phase Delay Versus the Ratio of AℓN Thickness to Wavelength

some value of t/λ ratio. As the curve indicates, an extrapolation of Liu's data predicted that for a t/λ of 0.7, the first order temperature coefficient of delay would go to zero. The maximum t/λ achieved at the time was 0.6. This is because at the lower frequencies (<500 MHz) of the previous performed measurements, the maximum growable AℓN film thickness (<5 μm) prevented the fabrication of high t/λ ratio delay lines. During TRW's investigation, delay lines with ratios as high as 1 were evaluated. As the TRW data (triangles) shows, the coefficient did not go to zero as expected, but rather reached an asymptotic value of 22 ppm/^{o}C.

2.4.4 Propagation Loss

The propagation loss of the AℓN/$Aℓ_2O_3$ was calculated to be about 27 dB/cm at 2 GHz. This value was obtained by first calculating the mismatch loss, adding to 6 dB bidirectional loss and then subtracting it from the measured insertion loss. Of course, the propagation loss depends greatly on the film quality and the substrate polish. However, most of the high quality film had relatively low propagation loss. This low value enables us to fabricate 2 GHz delay lines with unmatched insertion losses as low as 24 dB.

2.5 SAW OSCILLATOR DELAY LINE

Utilizing the data obtained from the previous study, especially the wave velocity dependence on t/λ, the delay line frequency can be adjusted by changing the AℓN thickness. A single mask allows adjustment of frequency in the order of 10 MHz at the 2.144 GHz operating frequency. Two delay lines were fabricated to be incorporated into the two deliverable oscillators required in this program. The delay line parameters are summarized in Table 2-2. The frequency response of the SAW 2 is shown in Figure 2-11.

Table 2-2. SAW Delay Line Data Summary

Parameter	SAW 1	SAW 2
Center Frequency	2.1789 GHz	2.145 GHz
Bandwidth (3 dB)	4.35 MHz	5.3 MHz
Untuned Insertion Loss	27.5 dB	28.5 dB

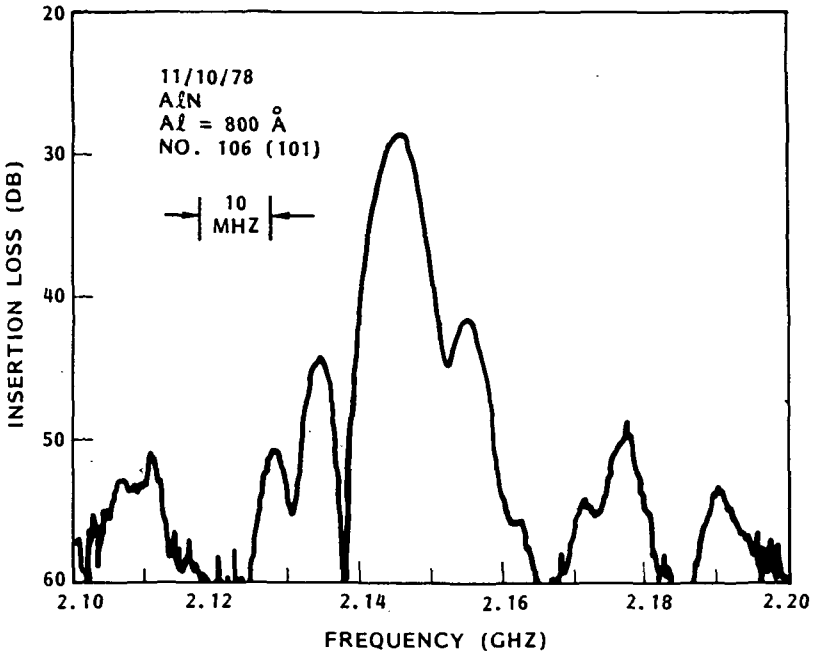

Figure 2-11. Frequency Response of Delay Line Used in the 2.144 GHz SAW Oscillator

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3. 2.14 GHZ SAW OSCILLATORS

Microwave SAW oscillators provide an attractive alternative to more conventional type oscillators for many applications. The 2.14 GHz SAW delay line oscillators fabricated for this program were designed for use as reference oscillators for a Ku-band source. The Ku-band reference source takes advantage of the SAW oscillator's characteristics which make them ideal microwave signal sources. The 2.14 GHz SAW oscillator microwave signal source provides a significant improvement in size, weight, and efficiency when compared to an equivalent multiplied bulk crystal source. The 2.14 GHz $A\ell N/A\ell_2O_3$ SAW delay lines were used as the frequency determining element in the fundamental mode oscillator. The high phase velocity 2.14 GHz SAW delay lines have significantly extended the upper frequency limit of SAW oscillators while retaining the frequency stability characteristics of lower frequency SAW oscillators.

3.1 OBJECTIVE

The objective of this task was to demonstrate and evaluate 2.14 GHz $A\ell N/A\ell_2O_3$ SAW delay line oscillators as a microwave signal source. This was accomplished as part of two programs, composed of the following tasks:

Phase 1:
- Design and fabrication of the basic 2.14 GHz $A\ell N/A\ell_2O_3$ SAW delay line oscillator
- Design and demonstration of an electronic temperature compensation circuit
- Characterization of the 2.14 GHz SAW oscillator and demonstration of its use as the reference oscillator in a Ku-band signal source.

Phase 2:
- Repackaging the 2.14 GHz SAW oscillator as a hybrid microwave integrated circuit (MIC)
- Characterization of the hybrid 2.14 GHz SAW oscillator and demonstration of its use as the reference oscillator in a Ku-band signal source.

3.2 SAW OSCILLATOR THEORY OF OPERATION

A SAW oscillator consists of a SAW delay line connected in a feedback loop with an amplifier as shown schematically in Figure 3-1. This circuit will oscillate at any frequency for which the total phase shift around the

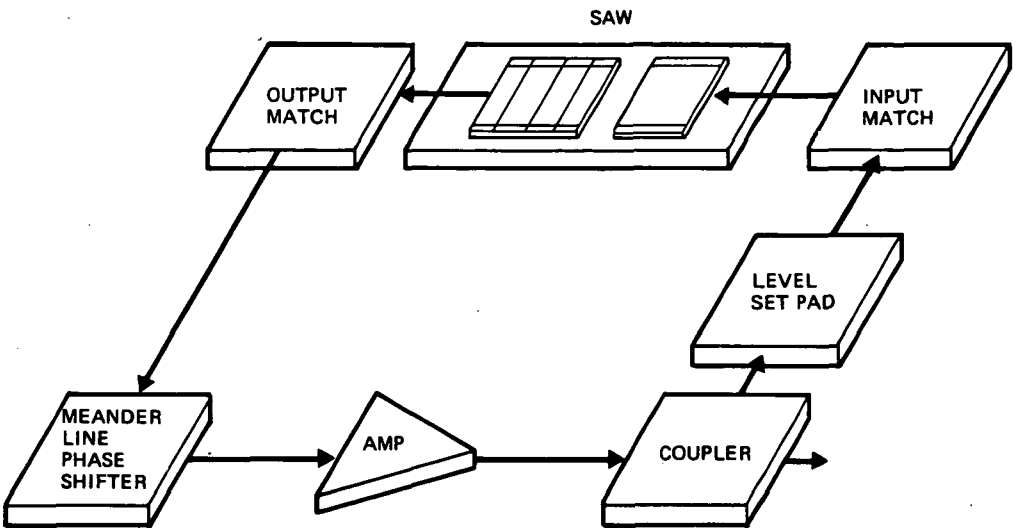

Figure 3-1. SAW Oscillator Functional Diagram

loop is an integer multiple of 2π, and the gain of the amplifier is equal to or greater than the net insertion loss of the feedback elements. The conditions for oscillation can be expressed as:

$$\frac{2\pi f \ell}{V} + \phi = 2n\pi \tag{3.1}$$

and

$$L_S(f) + L_1(f) = G(f, A) \tag{3.2}$$

where

f = oscillation frequency

ℓ = center to center transducer separation

V = surface wave velocity

ϕ = phase shift through all elements except SAW delay line

n = an integer

$L_S(f)$ = insertion loss of SAW delay line

$G(f, A)$ = amplifier gain as a function of f and output level, A

Solving (3.1) for f

$$f = \frac{V}{\ell}\left(n - \frac{\phi}{2}\right) \tag{3.3}$$

As a general rule, $L_1(f)$ and $G(f, A)$ are very slowly varying functions of f over a broad range around the frequency for which the oscillator is being designed, but $L_S(f)$ is a very strong function of frequency. The SAW delay is designed as a bandpass filter whose response is ideally given by

$$L_S(f) = K \left(\frac{\sin X}{X}\right)^2 \left(\frac{\sin Y}{Y}\right)^2 \tag{3.4}$$

where

$$X = \frac{2\pi N(f-f_o)}{f_o}$$

$$Y = \frac{2\pi M(f-f_o)}{f_o}$$

K = insertion loss at f_o

N = number of finger pairs in first transducer

M = number of finger pairs in second transducer

$$K\left[\frac{\sin\left(\frac{2\pi N(f-f_o)}{f_o}\right)}{\frac{2\pi N(f-f_o)}{f_o}}\right]^2 \left[\frac{\sin\left(\frac{2\pi M(f-f_o)}{f_o}\right)}{\frac{2\pi M(f-f_o)}{f_o}}\right]^2 = G(f_o, A) - L_1(f_o) \tag{3.5}$$

It is clear that the ideal case would be obtained when (3.3) is satisfied at f_o. Equation (3.3) has nearly n solutions, but the gain term of (3.5) can be adjusted such that the only simultaneous solutions to both (3.3) and (3.5) occur in the immediate vicinity of f_o. So long as only one solution to (3.3) falls within the primary response of the SAW delay line, single mode operation of the SAW oscillator is guaranteed.

It is also evident from (3.3) that some frequency modulation of the SAW oscillator is possible. Taking the derivative

$$\frac{df}{f} = \frac{-V d\phi}{2\pi\ell\phi} \tag{3.6}$$

This gives the expected result that the smaller the center to center transducer separation, i.e., the lower the delay line Q, the greater the SAW oscillator tuning range. The usual method of accomplishing the tuning or frequency modulation is via a varactor diode phase shift network.

The output phase noise density of the SAW oscillator can be expressed by

$$\text{Noise Power Density} = KT + NF + L + 20 \log \left[\sqrt{1 + \left(\frac{\omega_o}{2Q\Delta\omega} \right)^2} \right] \text{dBm/Hz} \qquad (3.7)$$

where

$KT = -174$ dBm/Hz

ω_o = the oscillator frequency

$L = L_1(\omega) + L_S(\omega)$

Q = the delay line loaded $Q(f_o/\Delta f_{3\ dB})$

$\Delta\omega$ = the offset frequency

Even when the bias conditions of the amplifier are carefully controlled, thermal noise and transistor noise will still result in oscillator phase and amplitude fluctuations. However, the phase noise component will generally dominate the amplitude noise. The noise power exhibits a floor at large offset frequencies which is determined by the amplifier noise figure and the delay line insertion loss. Minimum phase noise is achieved for minimum delay line loss, minimum amplifier noise figure, maximum filter Q, and maximum output power.

The preceding has established the design goals for the oscillator circuit, in particular equations (3.3), (3.5), and (3.7). The following discussion relates to the actual implementation of the circuitry surrounding the SAW delay line.

3.3 GHz SAW OSCILLATOR DESIGN CONCEPT

The 2.14 GHz SAW oscillator circuit functions, SAW delay line, gain blocks, and phase shifter were implemented using discrete component circuiting and standard commercial RF hybrids. Discrete circuitry assembled

on a duroid circuit board was used to realize the delay line matching circuits, the voltage-controlled and fixed phase shifters, and the temperature compensation circuitry. Standard commercially available hybrid packaged RF amplifier circuits were used to implement the oscillator gain blocks. The SAW delay line was housed in a sealed flatpack package.

All SAW oscillator circuitry is mounted on and interconnected by the duroid circuit board. The various discrete component circuit functions were fabricated directly on the duroid circuit board. The delay line matching circuit consisted of lumped element air core inductors which were resonated with the SAW delay lines internal shunt capacitance. The matching circuits transform the SAW delay line impedance to 50 ohms. The electronic phase shifter function was implemented using a voltage tuned bandpass filter. The phase shift through a bandpass filter varies across the bandpass of the filter; therefore as the frequency of the filter is changed, the phase shift at a specific frequency varies. The voltage tunable bandpass filter is a three-pole varactor tuned resonant line design fabricated directly on the duroid circuit board. The voltage tunable bandpass filter provides approximately 100 degrees of voltage-controlled phase shift within its bandpass.

The temperature control circuit was assembled on the duroid board using discrete components and conventional printed circuit assembly techniques.

The SAW oscillator circuit gain was realized using standard Avantek TO-8 packed RF amplifiers. One UTO-2311 and four UTO-2303 amplifiers are used in the 2.14 GHz SAW oscillator circuit. The low noise UTO-2311 amplifier is used as the low signal level point, at the output of the SAW delay line. The UTO-2311 has a noise figure of 5 dB over a frequency range of 1700 to 2300 MHz and has a gain of 8 dB. The UTO-2303 amplifiers are used to provide the remainder of the loop gain and to provide a high level buffered output port which minimizes loading effects on the oscillator. The UTO-2303 is a high level amplifier which has 8 dB of gain over the 1700 to 2300 MHz.

3.4 2.14 GHz SAW OSCILLATOR TEMPERATURE COMPENSATION CIRCUIT

The high phase velocity $A\ell N/A\ell_2O_3$ material used in the fabrication of the 2.14 GHz SAW delay lines has a greater temperature variation than ST-cut quartz. The temperature characteristics of the $A\ell N/A\ell_2O_3$ material are dependent on the T/λ ratio. In order to offset the $A\ell N/A\ell_2O_3$'s temperature variation, a temperature compensation technique was included in the 2.14 GHz SAW oscillator design.

Temperature compensation of the 2.14 GHz oscillator was accomplished with an active electronic circuit. The SAW oscillator is a voltage controlled design in which the frequency can be shifted by changing the voltage supplied to the electronic phase shifter. By applying an appropriate voltage to the frequency control input of the SAW oscillator, its frequency can be maintained constant with respect to varying temperature. A plot of the varactor tuning voltage required to maintain a constant oscillator frequency as the temperature is varied is shown in Figure 3-2.

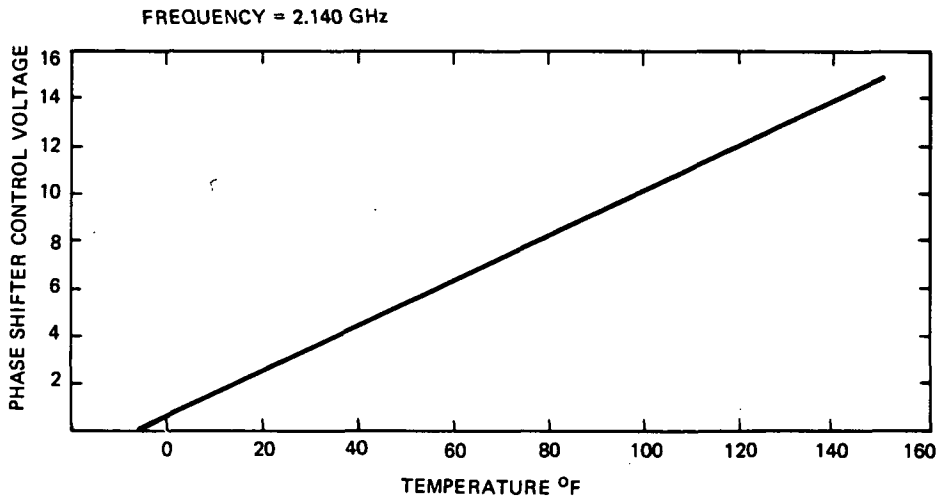

Figure 3-2. Phase Shifter Control Voltage Versus Temperature

A temperature compensation circuit generates the voltage-temperature function required to stabilize the SAW oscillator frequency over temperature. The temperature compensation circuit, shown in Figure 3-3, consists of a temperature sensing element (sensistor) which changes resistance with temperature. The varying resistance is converted to a voltage which is conditioned by an operational amplifier to generate the proper frequency

correction voltage. Figure 3-4 shows the temperature stability of a typical 2.14 GHz $A\ell N/A\ell_2O_3$ SAW oscillator with and without the electronic temperature compensation circuit. Over a frequency range of -20 to +140°F, the uncompensated SAW oscillator frequency varies 6 MHz. When the temperature compensation is applied, the frequency variation over the -20 to +140°F temperature range drops to 1.1 MHz.

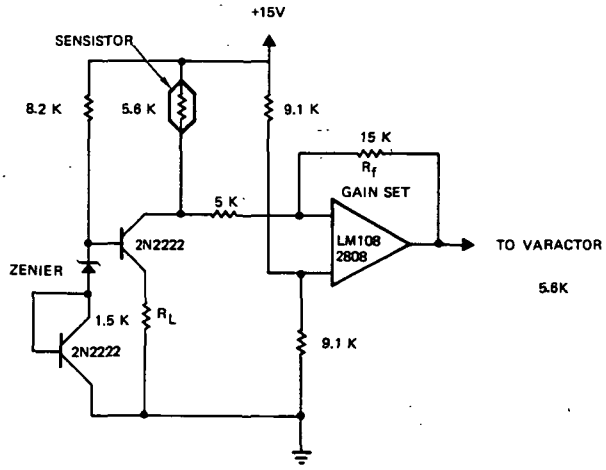

Figure 3-3. Temperature Compensation Circuit

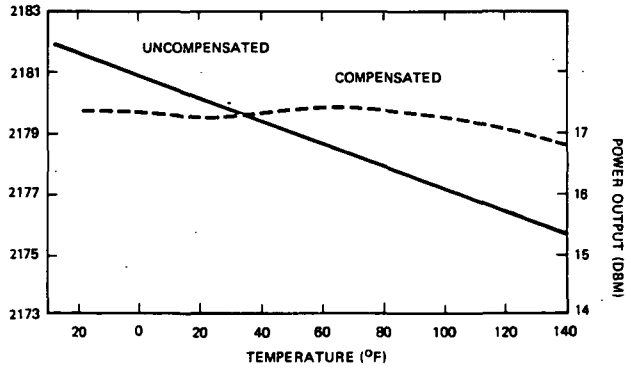

Figure 3-4. 2.14 GHz SAW Oscillator Temperature Characteristics

3.5 2.14 GHz SAW OSCILLATOR DETAILED DESIGN

A detailed block diagram of the 2.14 GHz SAW oscillator is shown in Figure 3-5.

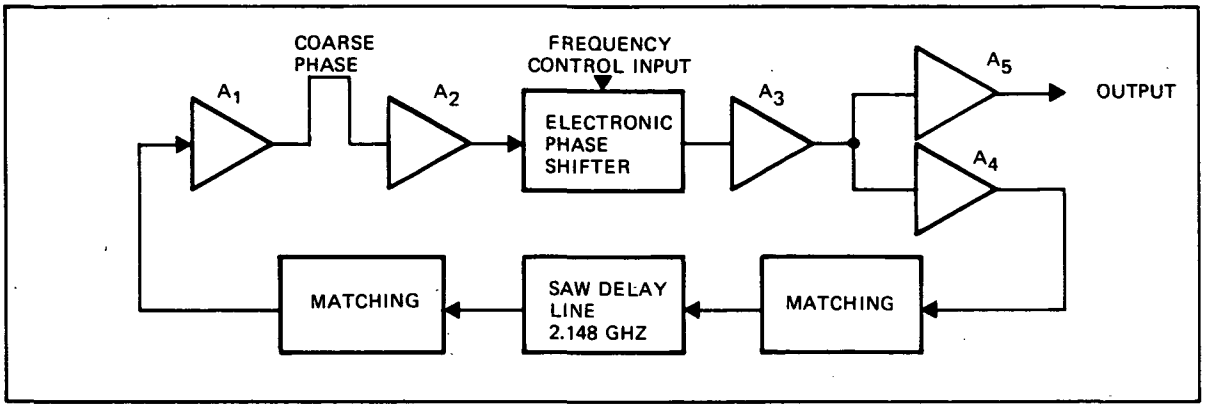

Figure 3-5. 2.14 GHz SAW Oscillator Block Diagram

The oscillator's feedback loop is formed by the SAW delay line, four Avantek TO-8 amplifiers, and the phase shifter bandpass filter. The output of the 2.14 GHz SAW delay line is matched to the 50Ω input impedance of the first loop amplifier, an Avantek UTO-2311, A1, with a lumped element series inductor. The UTO-2311 is a low noise figure amplifier used at the low signal level point at the output of the delay line to maintain the highest signal to noise ratio possible. The UTO-2311 amplifier has 8 dB of gain at 2 GHz and a 5 dB noise figure. The output of the UTO-2311 amplifier drives a selectable length of 0.020 inch diameter semirigid coaxial cable. The selectable coaxial cable is used to coarse set the total phase shift around the oscillator feedback loop to an integer multiple of 2π degrees. A UTO-2303 amplifier, A2, follows the coaxial line and provides an additional 8 dB of loop gain. The output of the A2 amplifier is coupled to the input of a three-pole varactor tuned bandpass filter.

The bandpass filter is used as a voltage controlled phase shifter. The filter consists of 3 resonant lines which were fabricated directly on the duroid circuit board. The filter is electronically tuned by capacitively loading the resonant lines with varactor diodes. The output of the filter is coupled to a second UTO-2303 amplifier, A3, which results in a circuit gain of approximately 22 dB at this point, three 8 dB amplifiers and approximately 2 dB of filter loss. The signal at the output of the second UTO-2303 amplifier is divided between the inputs of two UTO-2303 amplifiers A4 and A5. Amplifier A4 is in the feedback loop and its output is connected to the input of the SAW delay line. A4 is the high level

point of the feedback loop and operates in a gain compressed condition such that the net loop gain is unity. The other UTO-2303, A5, is the output buffer amplifier. The output buffer amplifier provides a high level output signal and isolates the SAW oscillator from output loading effects.

3.6 2.14 GHz SAW OSCILLATOR DATA SUMMARY

A summary of the 2.14 GHz SAW oscillators key performance parameters is shown in Table 3-1. The performance of the 2.14 GHz SAW oscillator is compared with the program design goals.

Table 3-1. 2.14 GHz SAW Oscillator Performance Summary

Parameter	Design Goals	Performance
Power Output	0 to +20 dBm	+17 dBm
Frequency	2.2 GHz	2.149
Frequency Settability	$\pm$0.15 3 dB BW	$\pm$0.20
Temperature Settability $0^{o}F$ to $120^{o}F$	$\pm$0.002%	$\pm$0.016%
Aging	1×10^{-8} pp day	2.25×10^{-6} pp day
Phase Noise dBc/Hz		
10 Hz		-16 dBc
100 Hz		-41 dBc
1 kHz		-73 dBc
10 kHz		-102 dBc
100 kHz		-126 dBc
1 MHz		-148 dBc

The temperature stability of temperature compensated SAW oscillator number 1 is $\pm$0.016 percent or $\pm$350 kHz over a 0 to $120^{o}F$ temperature range. Without temperature compensation, the oscillator frequency changes to $\pm$0.096 percent or $\pm$2.1 MHz over the same temperature range. The temperature compensation circuit improves the temperature stability of the 2.14

GHz $A\ell N/A\ell_2O_3$ SAW delay line oscillator by a factor of 6. The temperature stability of the number 2 SAW oscillator is ±300 kHz over the 0 to 120°F temperature range. The temperature performance data for the two 2.14 GHz SAW oscillators is summarized in Table 3-2 and Figures 3-6 and 3-7.

Table 3-2. 2.14 GHz SAW Oscillator Temperature Data Summary

Parameter	Oscillator 1	Oscillator 2
Frequency	2179 MHz	2148 MHz
Temperature Stability 0 to 120°F	±0.016%	±0.017%
Output Power	+16 dBm	+15.75 dBm
Output Power Variation	+0, -0.5 dB	+0, -0.6 dB

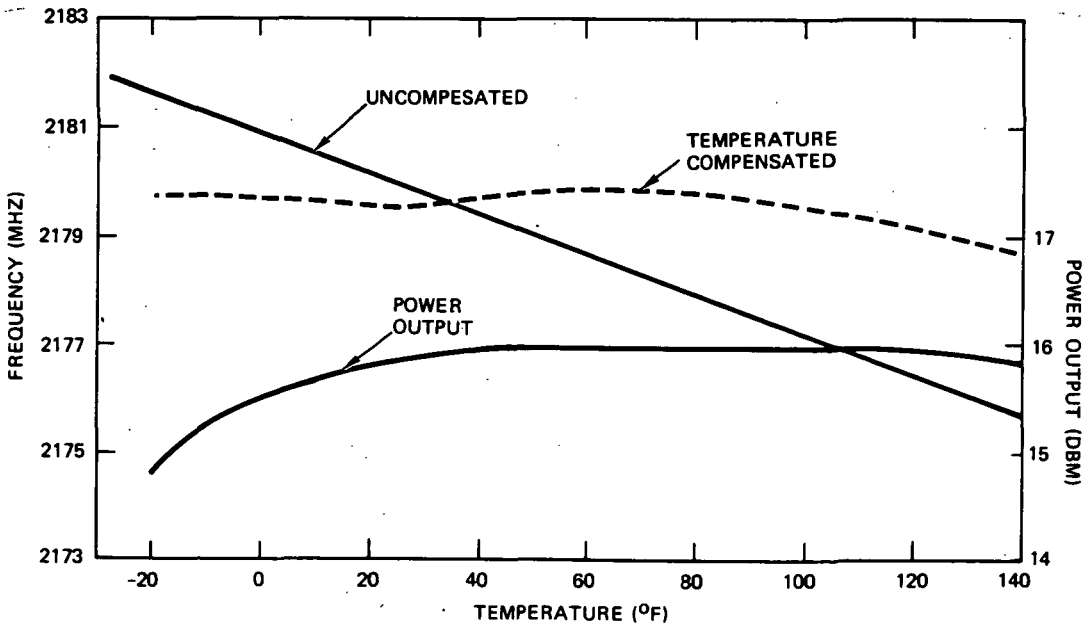

Figure 3-6. SAW Oscillator Number 1 Temperature Characteristics

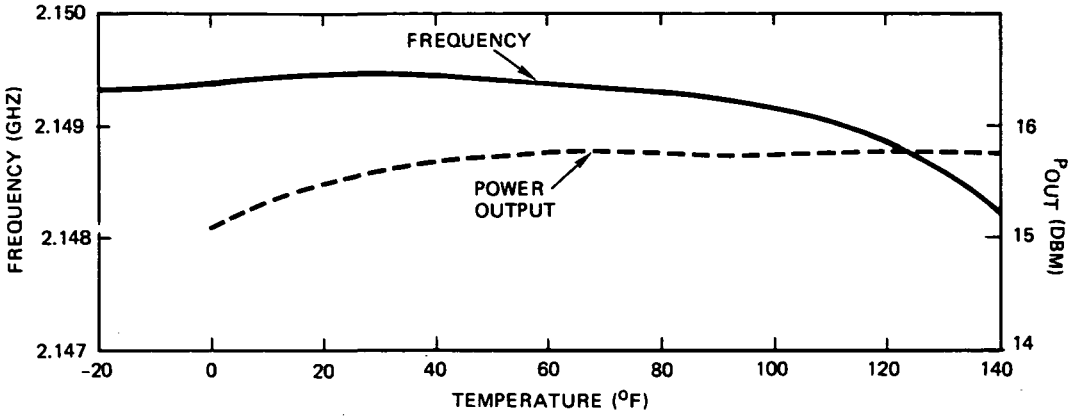

Figure 3-7. SAW Oscillator Number 2 Temperature Characteristics

The phase noise of the 2.14 GHz SAW oscillator was measured by TRW's metrology department. The measurement was made over the frequency range from 20 Hz to 1 MHz from the carrier. A phase noise plot of a typical 2.14 GHz SAW oscillator is shown in Figure 3-8. The oscillator phase noise exhibits a 20 dB per decade slope and has a noise floor of -160 dBc/Hz.

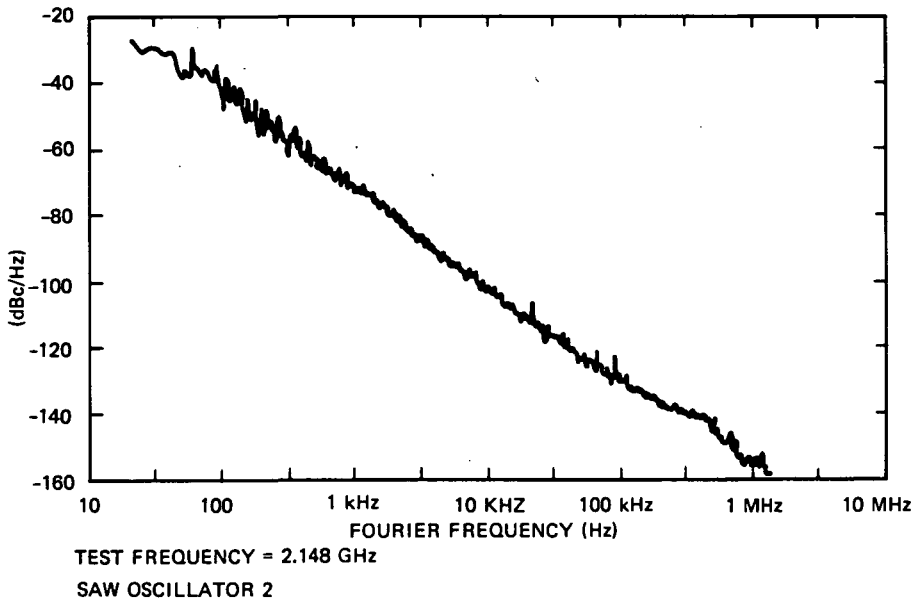

Figure 3-8. 2.14 GHz SAW Oscillator Phase Noise

3.7 2.14 GHz HYBRID PACKAGED SAW OSCILLATOR DESIGN CONCEPT

The 2.14 GHz hybrid packaged SAW oscillator is functionally similar to previous TRW designs. The SAW oscillator's circuitry was divided into two functional sections which were packaged separately. One hybrid package contains the $A\ell N/A\ell_2O_3$ SAW delay line, the matching circuits, and the electronic phase shifter. The second contains the 2 GHz amplifier circuitry. A coarse phase set coaxial line and level set attenuator which are used to control the oscillator's feedback characteristics are mounted external to the hybrid packages. The two hybrid packages with a minimum of external circuitry form a complete 2.14 GHz voltage-controlled SAW oscillator.

The SAW oscillator circuitry was configured as two hybrids for several reasons. The primary consideration in selecting a two package design is that special handling and cleaning procedures are required by the SAW delay line. This configuration places the active transistor amplifier circuitry and the SAW delay line in separate hybrid packages which can be assembled using techniques and processes which are optimum for the specific devices involved.

The two-package design significantly reduces the possibility of damage to the SAW delay line during the hybrid circuit alignment procedure. The amplifier circuit may require several iterative tuning operations during which the SAW delay line would be subject to damage if they were housed in the same package. The two-package concept also has the advantage that the amplifier hybrid which is a wideband design can be used with different SAW delay lines to build oscillators anywhere within the 1900 to 2600 MHz design range. The external phase shifter and level set attenuator allows any amplifier and delay line hybrid to be used in an oscillator assembly; they do not have to be built in a matched set.

3.8 2.14 GHz HYBRID PACKAGED SAW OSCILLATOR DETAILED DESIGN

A schematic diagram of the 2.14 GHz Hybrid packaged SAW oscillator is shown in Figure 3-9.

The majority of the 2.14 GHz hybrid packaged SAW oscillator circuitry is contained within the SAW delay line hybrid and the amplifier hybrid. The two hybrid packages and the external components used to set the feedback loop phase and amplitude are mounted on a duroid interconnect board.

The complete 2.14 GHz SAW oscillator assembly is housed in a 3.6 x 2.9 x 1.0 inch aluminum housing.

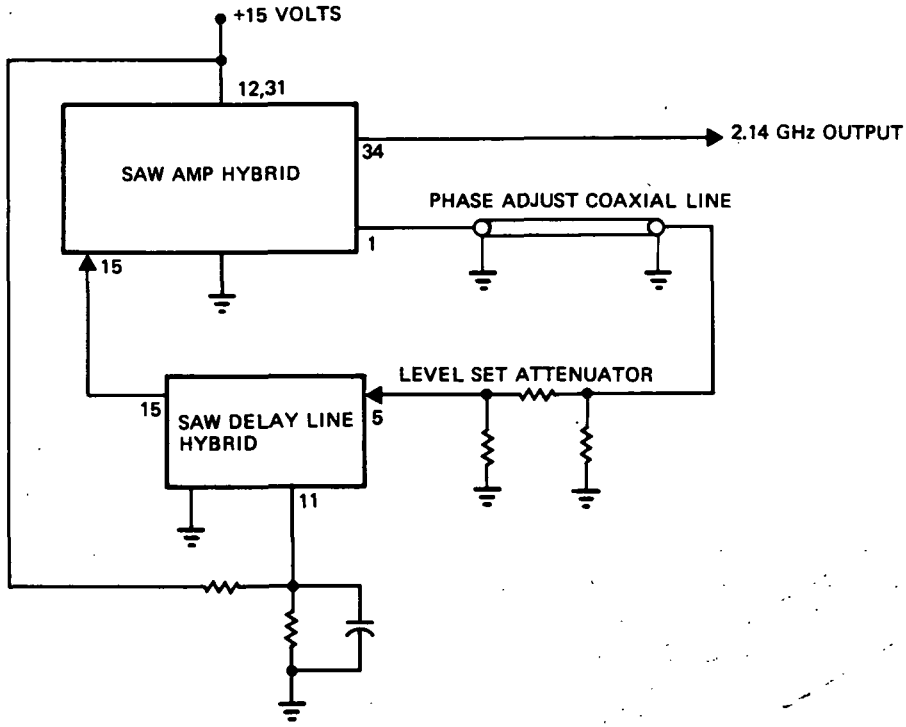

Figure 3-9. 2.14 GHz Hybrid Packaged SAW Oscillator Schematic

The 2.14 GHz oscillator's feedback phase shift is set by selecting the proper length of a 0.020 inch semirigid coaxial transmission line to provide the necessary feedback loop phase shift. The feedback loop level set attenuator is also placed external to the hybrid packages on the duroid interconnect board. The attenuation is provided by a resistive pad consisting of a network of discrete chip resistors. These are the only two circuit functions that are not contained within the two SAW oscillator hybrid packages.

A detailed schematic diagram of the 2.14 GHz SAW delay line hybrid is shown in Figure 3-10.

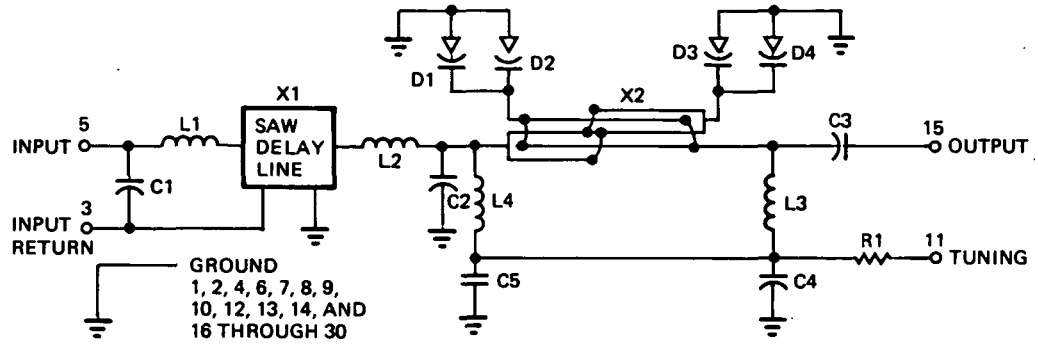

Figure 3-10. 2.14 GHz SAW Delay Line Hybrid Schematic Diagram

This hybrid contains all the circuit elements and functions which are directly related to the SAW delay line. The 50 ohm signal input to the hybrid is matched to the SAW delay line using an L section network consisting of a shunt input capacitance, C1, with a series inductance, L1, to the delay line. The output of the SAW delay line is transformed back to 50 ohms at the input of the phase shifter circuit using a second L network. The phase shifter consists of a 2 GHz Lange coupler, X2, which has its 90^{o} ports terminated with a variable reactance. The variable reactances (varactor diodes) phase shift and reflect the input signal back through the Lange coupler. The Lange coupler recombines the phase shifted signals which then appear at the output port. The varactor diodes, D1 through D4, are GHz Devices type GC1601 chip devices. The bias is applied to the varactor diodes via a pair of decoupling networks consisting of inductors L3, L4 and capacitors C4 and C5. The circuit is fabricated on a 0.025 inch alumina substrate. The 2.14 GHz SAW delay line circuit is housed in a 1.0 x 0.75 x 0.15 inch, 30 pin Tekform 50112 package.

A block diagram of the 2 GHz SAW amplifier is shown in Figure 3-11.

The 2 GHz SAW amplifier hybrid contains five amplifier stages and a Wilkenson power divider. Four of the amplifier stages are part of the SAW oscillator's feedback path and provide approximately 30 dB of loop gain. The amplifiers have been configured using two-stage designs consisting of two cascaded Hewlett-Packard HXTR 5001 transistors on each substrate.

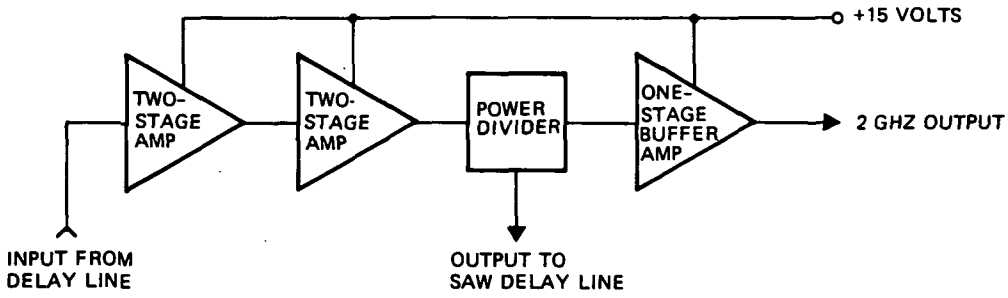

Figure 3-11. 2 GHz SAW Amplifier Block Diagram

The amplifier was designed using CAD (computer-aided design) procedures and uses conventional RF circuit techniques. Each transistor uses gain compensating feedback in addition to broadband input and output matching circuits to achieve the desired bandpass characteristics. Then each is biased using an active bias network consisting of two 2N2907 transistors and an LM113 precision voltage reference. Two of the two-stage amplifier substrates are cascaded to provide the 30 dB of feedback loop gain. The output of the four-stage amplifier is power split by a Wilkenson 3 dB power divider. One side of the power divider provides the signal for the SAW oscillator's feedback loop. The second power divider output drives the input to a one-stage output buffer amplifier. The output buffer amplifier is the output half of the two-stage cascaded circuit and uses the HXTR 5001 transistor to provide a +8 dBm output level.

3.9 2.14 GHz HYBRID PACKAGE SAW OSCILLATOR DATA SUMMARY

A summary of the 2.14 GHz hybrid packaged SAW oscillator's key performance parameters are shown in Table 3-3. The performance of the 2.14 GHz hybrid packaged SAW oscillator is compared with the program design goals. The temperature stability of the hybrid packaged oscillators is $\pm$0.104%. It should be noted that the hybrid package 2.14 GHz SAW oscillator does not have an electronic temperature compensation circuit. Figure 3-12 is a plot of the temperature characteristics of the SAW oscillator. The frequency varies from 2.1492 to 2.1447 GHz over a -20^{o}C to 50^{o}C temperature range, while the output power remains within $\pm$0.4 dB of the +8.2 dBm level.

Table 3-3. 2.14 GHz Hybrid Packaged SAW Oscillator Data Summary

Parameter	Design Goal	Performance
Power Output	0 to +20 dBm	+8 dBm
Frequency	2.2 GHz	2.147 GHz
Frequency Settability	±0.15, 3 dB BW	±0.2
Temperature Settability	±0.002%	±0.104%
-20 to 50°C		
Phase Noise dBc/Hz		
100 Hz		-34 dBc
1 kHz		-62 dBc
10 kHz		-90 dBc
100 kHz		-112 dBc
1 MHz		-132 dBc

The phase noise of the 2.14 GHz hybrid packaged SAW oscillator was measured by TRW's metrology department; the measurements were made over a frequency range from 20 Hz to 1 MHz from the carrier. A phase noise plot of a hybrid packaged 2.14 GHz SAW oscillator is shown in Figure 3-13. The oscillator phase noise exhibits a 20 dB per decade slope, and the measurement setup has noise floor approximately 20 dB below the measured data.

3.10 2.14 GHz SAW OSCILLATOR DATA COMPARISON

The electrical performance of the temperature compensated SAW oscillator and the hybrid packaged SAW oscillator differs in two major areas. The first difference is that the hybrid version of the SAW oscillator does not have the active temperature compensation. The temperature compensated oscillator has a stability of 5.6×10^{-6} ppm/°C while the uncompensated oscillator has a stability of 3×10^{-5} ppm/°C. Figure 3-13 is a plot of the temperature characteristic of the two oscillators.

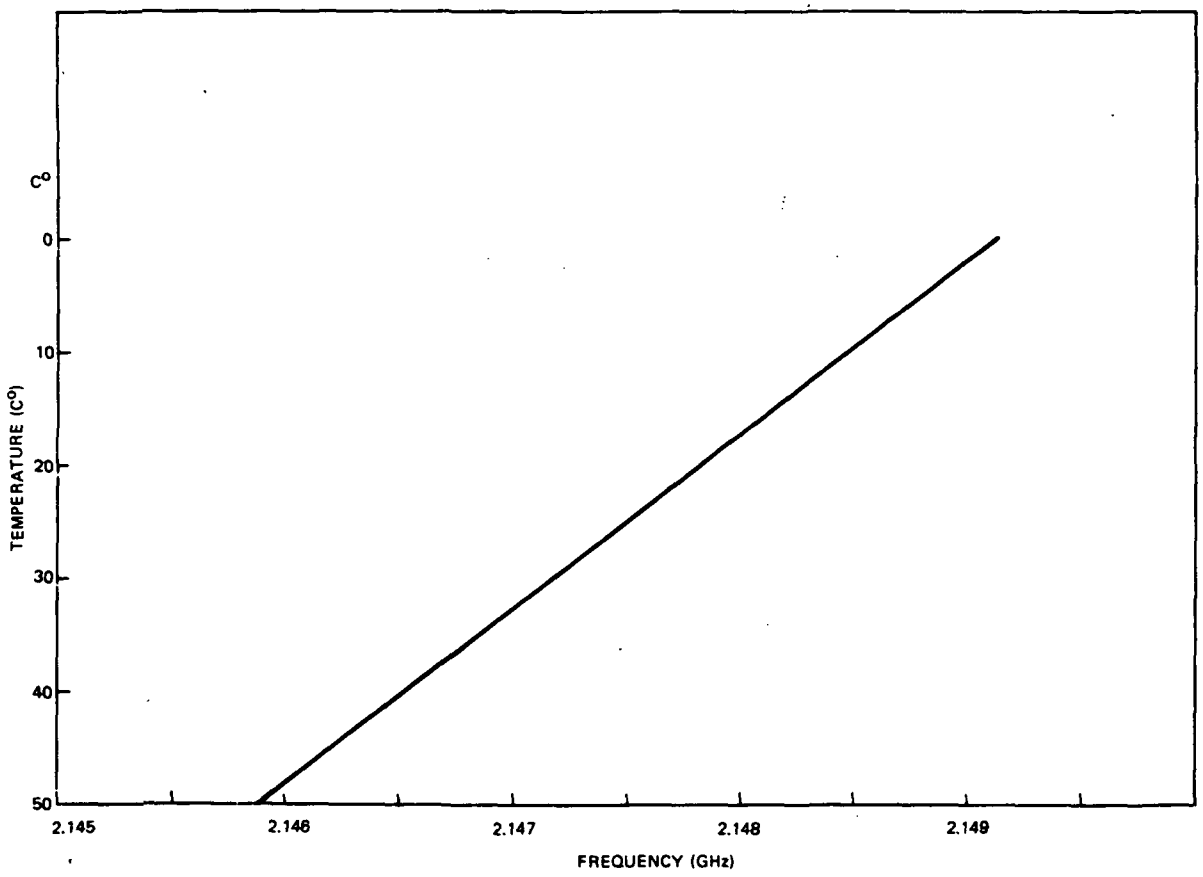

Figure 3-12. 2.14 GHz Hybrid Packaged SAW Oscillator Temperature Characteristics

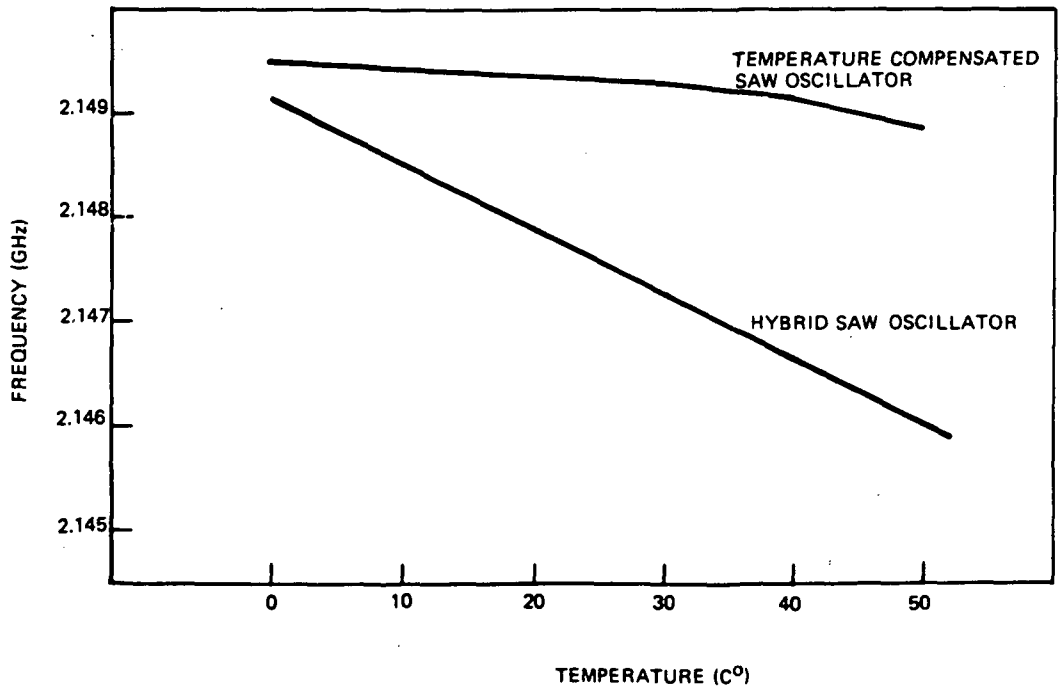

Figure 3-13. 2.14 GHz Hybrid Packaged SAW Oscillator Temperature

The second area of major performance variation is the phase noise characteristic. There are several factors that affect the phase noise and account for the majority of the difference in phase noise performance. The phase noise characteristics of the two oscillators are shown in Figure 3-14. The noise power density of a SAW oscillator can be expressed by:

$$\text{Noise Power Density} = KT + NF + L - PO + 20 \log \left[1 + \frac{\omega_o}{2Q_{\Delta\omega}}\right]^2 \text{ dBm/Hz}$$

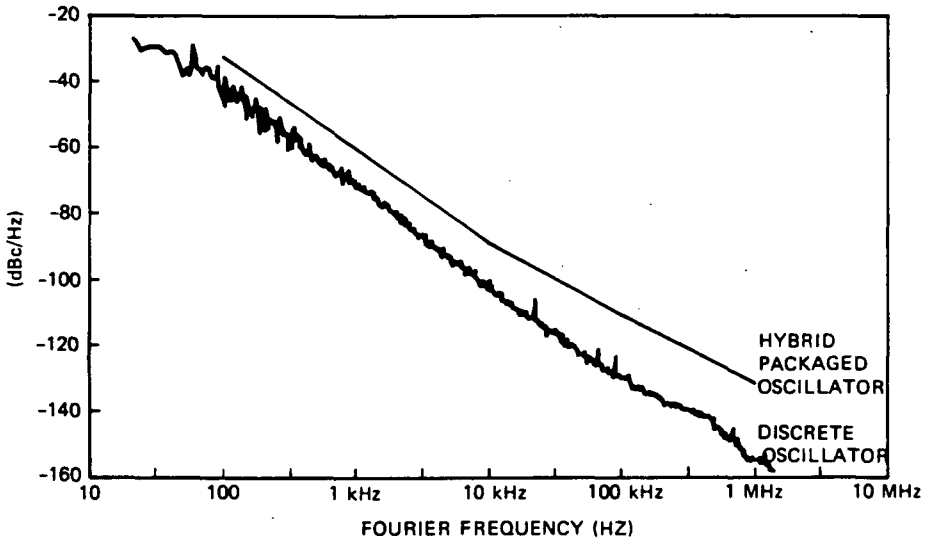

Figure 3-14. 2.14 GHz SAW Oscillator Phase Noise Comparison

where

KT = -174 dBm/Hz

ωo = oscillator frequency

$L = L_1(\omega) + L_s(\omega)$

Q = delay line loaded Q

$\Delta\omega$ = offset frequency

PO = output power

For the 2.14 GHz temperature-compensated SAW oscillator and the hybrid packaged SAW oscillator, the values of ωo, L, and Q are similar, which should result in comparable phase noise performance. The output level of the hybrid packaged oscillator is +8 dBm, 9 dB less than the +17 dBm output level of the temperature compensated SAW oscillator. The 9 dB difference in the oscillator's output power is responsible for the majority of the phase noise difference, approximately 10 dB at 1 kHz.

4. TED DIVIDER

The TED divider is a device capable of coherently dividing a microwave signal. The TED operates at frequencies much higher than conventional frequency dividers, in this case a divide-by-seven at 15 GHz. The 15 GHz divide-by-seven circuit provides a very attractive way of implementing a phaselocked Ku-band frequency source. The basic TED divider circuit is very simple and small in size when compared to the alternate approach, a X7 multiplier. The potential advantages the TED divider offers in frequency source applications could significantly simplify many microwave circuit designs.

4.1 OBJECTIVES

The objective of this effort was to design and fabricate a TED divider circuit suitable for use in a 15 GHz phase locked frequency source. To accomplish this goal, the following tasks were addressed during the course of two programs.

Phase 1:
- Design and fabricate TED devices
- Evaluate TED devices as frequency dividers
- Identify problem areas.

Phase 2:
- Optimize TED device design
- Design, fabricate, and demonstrate a TED temperature compensation technique
- Use the TED divider in the Ku-band phaselocked frequency source.

4.2 TED THEORY OF OPERATION

The TED is a TRW-developed n-type GaAs TED triode. The triode structure is formed by adding a gate structure between the TED anode and cathode terminals. The output frequency of the TED is determined by the electrical length (transit time) between the anode and cathode of the device. An electron domain initiated at the cathode travels along the length of the device to the anode. The travel time of the domain determines the output frequency of the device. When an electron domain has been formed, another domain cannot be initiated until the domain in transit reaches the anode.

Therefore, if the TED device is biased so that new domains are initiated by the injection of a signal into the gate structure, the device can be used as a frequency divider because the TED will not react to trigger pulses during its transition time. In the case of the 15 GHz divider, the six input pulses which are applied during the transition time do not initiate a new electron domain. The seventh pulse, which is applied after the domain has arrived at the anode, reinitiates a new electron domain at the cathode. Figure 4-1 is a photograph of a TED device showing the anode, cathode and gate structures. Figure 4-2 is a TED divider circuit diagram showing how the TED is used as a frequency divider.

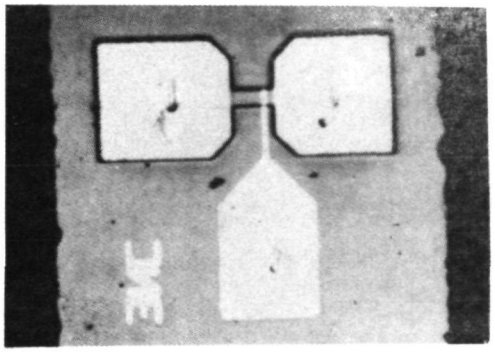

Figure 4-1. 2.144 GHz TED

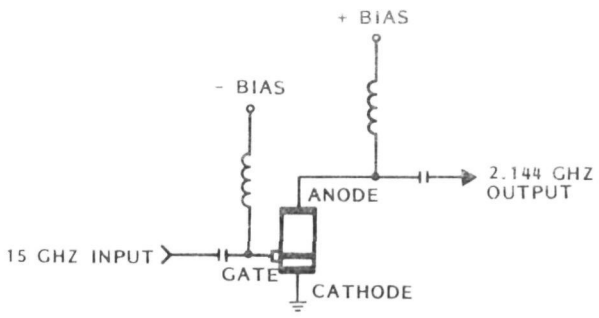

Figure 4-2. TED Divider Circuit

4.3 TED DEVICE DESIGN

The basic design of TED's as reported in the literature expresses the frequency of operation in terms of the transit length, ℓt, and the saturation velocity Vo, as:

$$F = \frac{\bar{V}_o}{\ell_t}$$

Another empirical relationship by Claxton[2] et al., suggests that the frequency term include the low field mobility as:

$$F = \frac{1.27\ 10^7}{\ell_t} \times \frac{\mu_o}{8000}$$

Investigations on a TRW funded program indicate that the frequency of oscillation may vary with concentration, contact resistance, and anode and gate bias. A developed mode suggests that the transit length varies as the width of the stationary domain, which is launched at the gate.

The model considers the device divided into three sections, as indicated below in Figure 4-3. The low field region between the gate and cathode is region I, the region under the gate depletion is region II, and the transit length from gate to anode is region III.

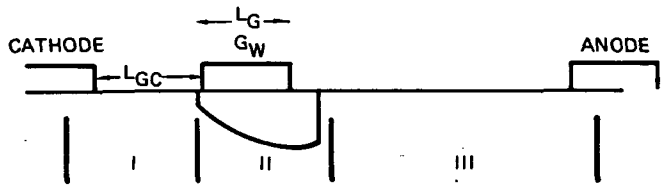

Figure 4-3. TED Model

The anode to cathode bias, V_{AC}, is then the sum of the voltage drop across the three regions, and is given by:

$$V_{AC} = V_I + V_{II}\ V_{III}$$

This analysis is used to design for a given frequency and the power dissipation.

Because there is a minimum field requirement for the transit region, V_{III} may be considered fixed for a certain frequency and Nd product. The power dissipation, P_d, may be given as the product of the threshold voltage V_{th} and the peak current, where

$$P_d = (V_I + V_{II} + V_{III}) \times I_p$$

P_d can be minimized by minimizing V_I, V_{II}, and V_{III}. The primary approach is to make the active channel in region III as narrow as possible, and the thickness of the active layer, d, in this region as thin as is consistent with achieving differential negative resistance. An Nd product of >1 x 10^{12} cm^{-2} must be maintained. The lower limit on the channel width is 10d to allow the domain to form. Additionally, the dissipation in region I and region II may be minimized by minimizing ℓ_g and ℓ_{g-c}. The lower limit on ℓ_g is ℓ_g > 3d to avoid rounding of the entire depletion region. The limit on ℓ_{g-c} is dependent upon the minimum geometry that can be resolved with photolithographic processes. Typical values used in our designs are shown in Figure 4-4.

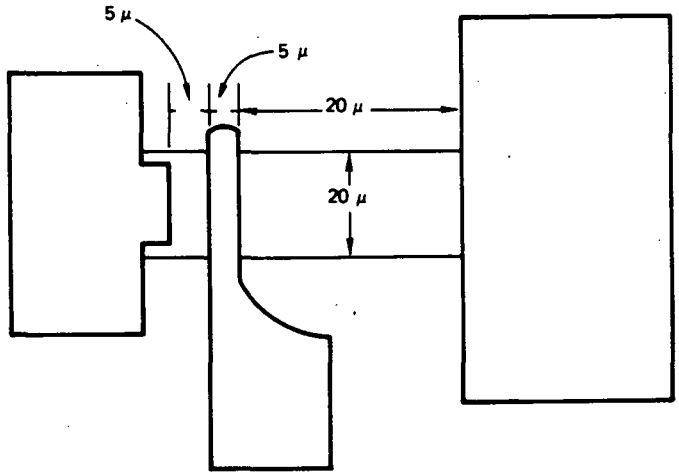

Figure 4-4. TED Geometry

Using the TED model, for a given N_0d_0 and a given f_0, a slight increase in N_0d_0 causes f_0 to increase. This has been verified experimentally. Additionally, the oscillation frequency has been shown to vary with gate and anode bias. A slight decrease in power dissipation is possible if the Nd product is trimmed to a minimum and the correct bias conditions are chosen.

When designing for a minimum power dissipation, the magnitude of the current swing during oscillation should not be ignored. Because V_{AC} is relatively constant for a desired frequency, the channel width will determine the current flow, for both the dc and the small signal cases. To minimize the current, the channel should be as narrow as possible.

For a given N_d and fixed L_g and L_{gc}, V_I and V_{II} are independent of the channel width. However, to reduce V_I and V_{II}, L_g and L_{gc} must be reduced.

The lower limit on the channel width is 10d to allow the domain to form. The reduction of L_g and L_{gc} is in part dependent on the state of the art of photolithography. Additionally, L_g should be greater than 3d to avoid rounding of the depletion region, which would make domain nucleation more difficult.

The material parameters are determined using the computer program for a given frequency, anode to gate spacing, and biasing conditions. The program uses the transit length variation as of function of N_d and bias to determine the frequency.

4.4 MATERIALS TECHNOLOGY

4.4.1 Introduction

All TED devices developed in this program were fabricated with GaAs epitaxial wafers grown at TRW. Although the GaAs material development was not a part of this device study, the techniques employed in growing and characterizing the epitaxial wafers will be described in this section for completeness.

4.4.2 Epitaxial GaAs Deposition

The epitaxial layers were deposited in a vapor phase, vertical deposition system employing AsH_3, Ga, and HCl as its principal reactants. The epitaxial system is shown in Figure 4-5 and consists of a five-zone furnace, a reactor tube, and a gas flow control system. Zone one preheats the entry gases and zone two maintains the Ga reservoir at the desired temperature. Zone four is the region where epitaxial layer deposition takes place, while zone three and zone five are buffer zones for temperature stabilization at zones two and four.

The resistance heated furnace is split and operates in a clamshell motion which aids in rapid cooling of the deposition chamber. The furnace is equipped with heat shields which cover each half of the furnace. These

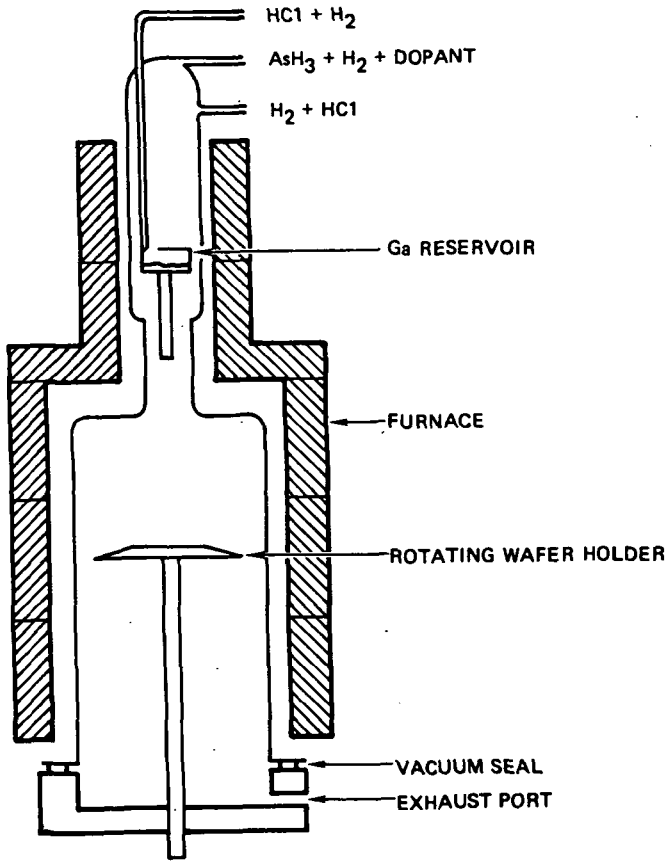

Figure 4-5. Schematic of EPI Reactor

serve to establish an equilibrium temperature in the furnace prior to locking the two halves around the reactor tube, permitting the deposition chamber to be brought rapidly to the desired deposition temperature. This minimizes outdiffusion of dopants from the substrate during the time the wafer is being brought up to the deposition temperature. The reaction tube has three entry ports for introducing the reaction gases. One port contains the Ga reservoir, through which HC1 is passed to form $GaCl_3$. A second port is used for AsH_3 and H2, and the third port is used for HC1 and H2 for etching and control of the background doping concentration. The deposited layer may be doped with sulfur by the introduction of H_2S at the second port.

4.4.3 Chemistry of Epitaxial Growth

Epitaxial growth in an arsine reactor occurs by a sequence of reversible chemical reactions as follows:

a) Formation of GaCl at the Ga reservoir

$$3\ HCl + 3\ Ga \rightleftarrows 3\ GaCl + \frac{3}{2}\ H_2 \qquad (4.1)$$

b) Decomposition of arsine gas to arsenic vapor at high temperature

$$2\ AsH_3 \rightleftarrows \frac{1}{2}\ As_4 + 6\ H_2 \qquad (4.2)$$

c) Epitaxial growth of GaAs on the substrate

$$\frac{1}{2}\ As_4 + 3\ GaCl \rightleftarrows 2\ GaAs + GaCl_3 \qquad (4.3)$$

In the absence of impurities, reactions (4.1) through (4.3) would lead to undoped GaAs films. It has been shown, however, that Si is a major background impurity in quartz reactor systems. According to DiLorenzo* chlorosilanes may be produced by high temperature reactions of H_2 and HCl with the quartz tube.

$$nHCl + (4-n)\ H_2 + SiO_2 \rightarrow SiCl_nH_{4-n} + 2\ H_2O \qquad (4.4)$$

for n = 1, 2, 3, and 4. At the substrate Si may be incorporated in the epitaxial film as a background dopant, as follows

$$(n-2)\ H_2 + SiCl_nH_{4-n} \rightarrow Si + nHCl \qquad (4.5)$$

*J.V. DiLorenzo, "Vapor Growth of Epitaxial GaAs: A Summary of Parameters Which Infouence the Purity and Morphology of Epitaxial Layers," Journal of Crystal Growth, Vol. 17, pp 189-206, (1972).

This reaction can occur simultaneously with (4.3) and represents doping of the epitaxial film with Si. The activity of Si incorporation is given by

$$a_{Si} = K_n \frac{P_{SiCl_nH_{4-n}}}{P^n_{HCl}} \tag{4.6}$$

Where the K_n represents the various equilibrium constants of reaction (5), and the P's are the partial pressures of the constituents which are proportional to the mole fractions. Thus the unintentional doping by Si is inversely proportional to the partial pressure of HCl in the reactor. DiLorenzo's studies of this phenomenon were undertaken in a reactor using $AsCl_3$ in which the HCl partial pressure depends upon the $AsCl_3$ mole fraction from the reaction

$$3\ H_2 + 2\ AsCl_3 \rightleftarrows \frac{1}{2}\ As_4 + 6\ HCl \tag{4.7}$$

He verified the marked inverse dependence of the impurity concentration on the $AsCl_3$ mole fraction.

In the arsine reactor of the present study, the HCl mole fraction may be increased directly by increasing the partial pressure of HCl in the third input port of Figure 4-5. By this method it has been possible to consistently grow undoped GaAs films with free carrier concentrations less than 10^{13} cm^{-3}.

Materials for particular applications are prepared by intentionally doping with sulfur to the required concentration by controlled introduction of H_2S into the reactor during growth. Doped epitaxial films with free carrier concentrations ranging from 10^{15} -2 x 10^{17} cm^{-3} have been prepared for different applications. Materials prepared for fabrication of devices in this study employed concentrations from 1015 -2 x 10^{16} cm^{-3}.

4.4.4 Characterization of GaAs Epitaxial Material

The techniques used to characterize the GaAs materials used in this study have been developed and refined over a period of several years. The

standard characterization methods include Hall measurements, concentration profiling by capacitance-voltage methods, surface examination and thickness measurement.

4.4.4.1 Hall Measurements

The mobility μ and carrier concentration n are determined in a magnetic field of 5 kG by the van der Pauw method. The Hall mobilities of materials grown at TRW are plotted in Figures 4-6 and 4-7 as a function of free carrier concentration at measurement temperatures of 300 and 77°K respectively. These points are superimposed in the figures on curves given by Rode and Knight* for experimental values of Hall mobilities and theoretical values of the electron drift mobility. Compensation ratios, δ, (the ratio of ionized impurity concentration to free electron concentration) of one and two have been used for the two theoretical curves shown. At 300°K, the error in comparing Hall mobility and electron drift mobility is small. The epitaxial materials grown at TRW compare very favorably with the material grown at other laboratories (the experimental line) and indicate a compensation factor of about 2 for the unbuffered material. This result could only be achieved in high quality films since the compensation ratio, estimated in this manner, is also a measure of the point defects in the crystal.

4.4.4.2 Doping Concentration and Layer Depth Measurements

The doping concentration of the active layer is determined from the I-V data in the Hall mobility measurement and substantiated with a differential capacitance-voltage technique. The capacitance-voltage measurement of a Schottky diode on the material gives both concentration and epitaxial layer depths. The concentration is expressed as

$$M = \frac{C^3 dv}{A^2 dC \epsilon \epsilon_0 q}$$

*D.L. Rode and S. Knight, "Electron Transport in GaAs," Phys. Rev. B, Vol. 3, No. 8, pp. 2534-41, (15 April 1971).

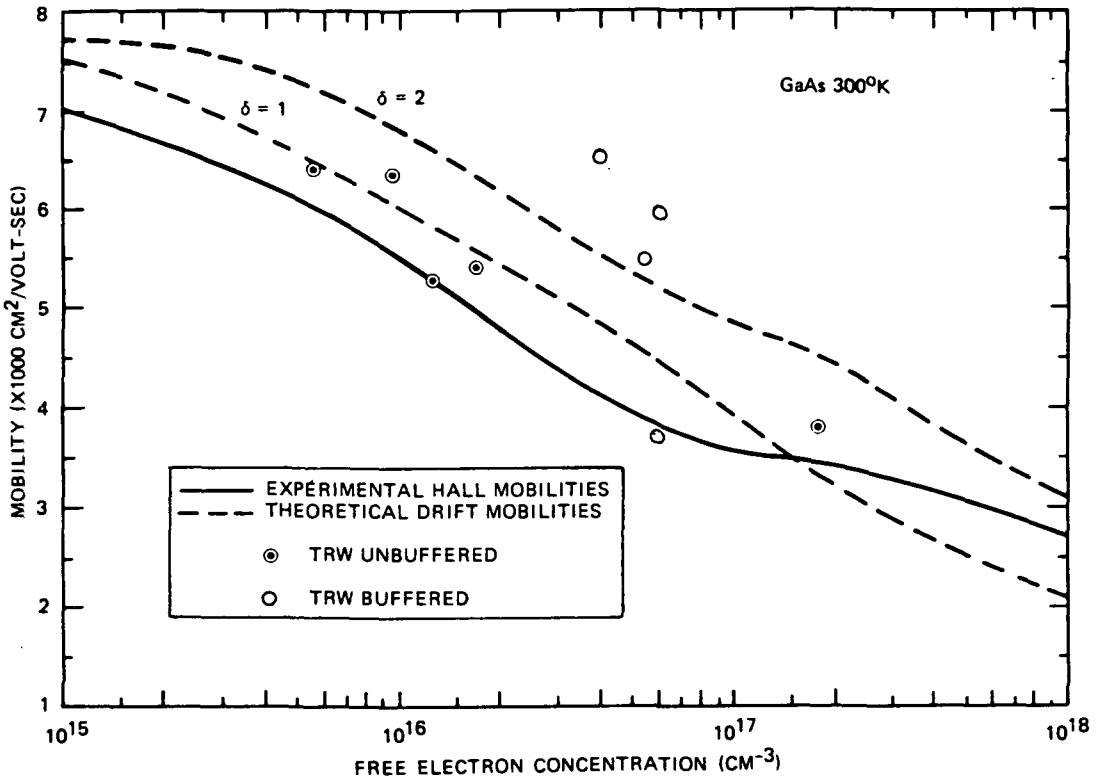

Figure 4-6. Free Electron Concentration

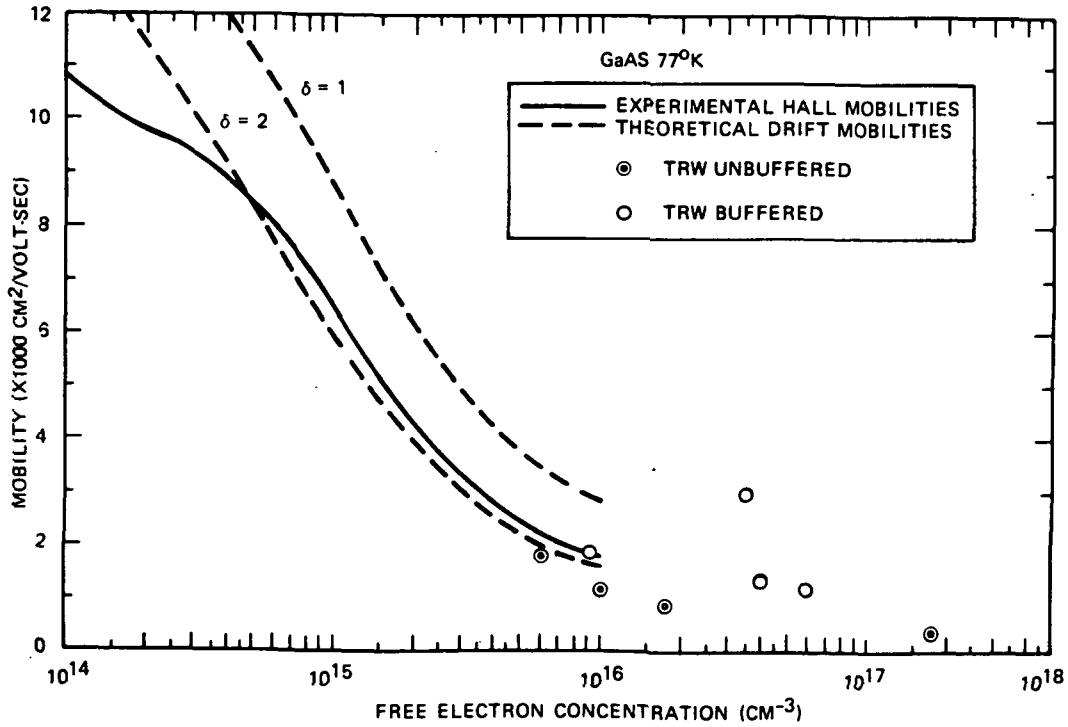

Figure 4-7. Free Electron Concentration

where the capacitance C is the average of two differential capacitance measurements, ϵ is the dielectric constant, ϵo the permittivity of free space, q the electronic charge, and A the diode area.

The variation of the diode capacitance with applied voltage is used to determine the electrical thickness of the epitaxial layer. The depletion spreading is expressed as

$$X = \frac{\epsilon \epsilon_o A}{C}$$

The electrical depth is determined arbitrarily as the point where the doping concentration is reduced by a factor of two. The C-V data is computed and plotted automatically on a profiler. The C-V method of thickness measurement is limited by the fact that the Schottky barrier diode breakdown voltage is sometimes lower than the pinch-off voltage. In such cases, the mechanical layer thickness is determined by a groove and stain technique. It should be noted that the electrical thickness can be appreciably less than the mechanical thickness due to out diffusion of Cr from the substrate into the epitaxially deposited layer.

4.5 TED FABRICATION PROCESS

A flow diagram of the standard fabrication process is illustrated in Figure 4-8. The various processing steps were basically developed on other programs and have been discussed in previous reports (1, 2). The key steps directly relating to developing devices for the 2.144 GHz application are also discussed here. These include the materials, the ohmic contacts, and the device characterization.

The process sequence begins with an epitaxial wafer of the desired thickness and concentration, shown in Table 4-1.

An epitaxial layer thickness of $\sim$1 μm and a concentration of 2×10^{16} was chosen to given an Nd > 10^{12} cm^{-2}. This Nd product relationship seems to be necessary to achieve differential negative resistance.

The active epitaxial layer was also deposited onto a semi-insulating epitaxial buffer layer. The buffer layers, which are deposited on Cr doped substrates, were necessary to achieve differential negative resistance when

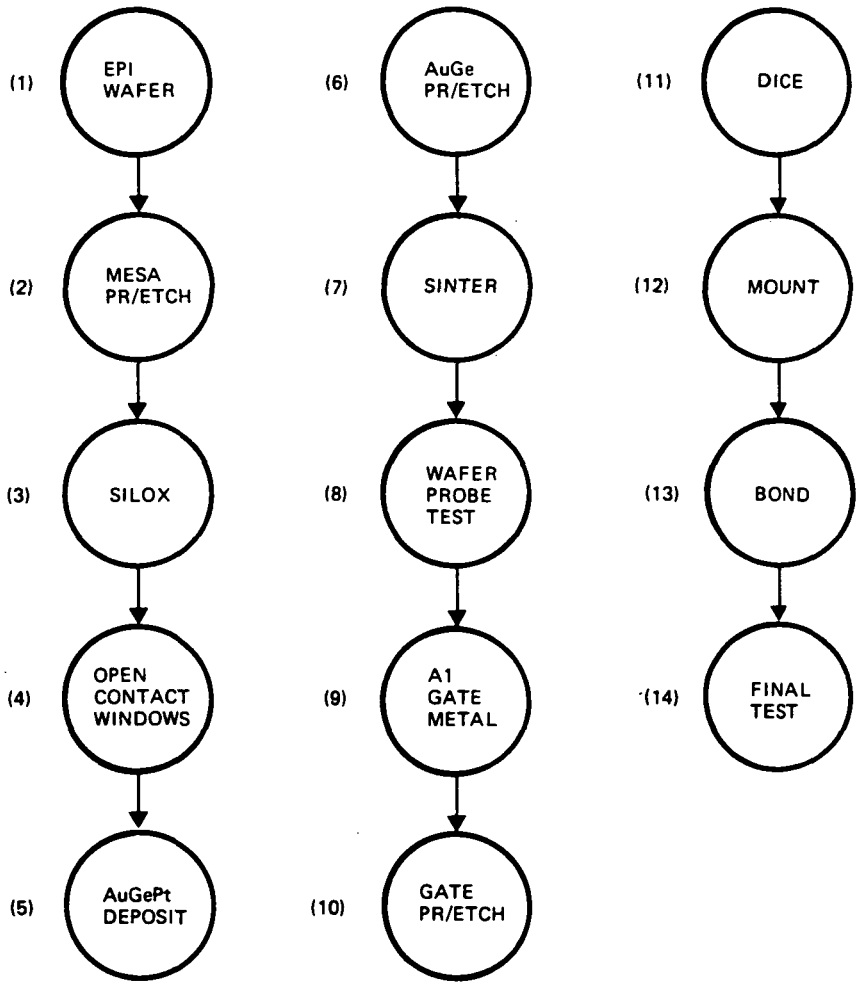

Figure 4-8. Standard Processing Sequence of this Study

Table 4-1. GaAs Material Used for TED Fabrication

EPI No.	Thickness (μm)	N_D (ATOMS-cm^{-3})	Hall Mobility $\frac{cm^2}{VOLT\text{-}SEC}$	TED Run No.
1430	0.9	2.2×10^{16}	6400	T-2-1
1430	0.75	2.2×10^{16}	6400	T-2-2

low Nd product values (near 10^{12} cm^{-2}) were used. Devices are isolated on the wafer by etching mesas, which are formed by using a photolithographic masking technique followed by an anisotropic etch. A typical mesa with good gate coverage is shown in Figure 4-9.

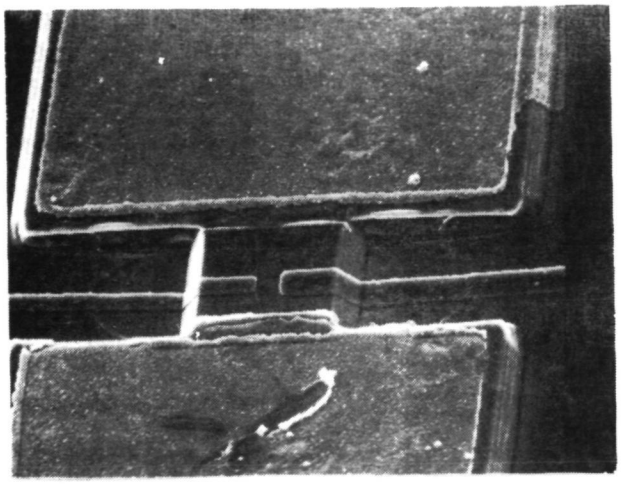

Figure 4-9. SEM Photograph

A gold-germanium alloy contact is used at the anode and cathode. The germanium from this alloy mixture provides n-type doping for the GaAs in the contact region. A platinum and gold layer or a thick gold layer is used over the AuGe contact to provide sufficient metallization for thermo-compression bonding.

The gold-germanium is deposited sequentially, or as a eutectic mixture. When the contact metallization is applied, silox is used as a protective covering over the entire wafer except in the contact regions to prevent contamination of the channel or mesa areas. After the contacts are sintered, the Gunn devices are characterized prior to gate metallization. The gate metal is deposited and then delineated using a photolithographic technique. After the gates are delineated, they are sintered at 300°C.

The mounting and bonding of the devices are dependent upon the particular application. In the standard mounting technique, the wafers are thinned to a thickness of ~5 mils, and a gold metallization evaporated on the backside of the wafer. The wafer is then mounted to the test fixture or circuit using either a silver conducting epoxy or by eutectic mounting.

In this specific case, the mounting was varied to control the heat dissipation to specific values. Because it was determined that a broader tuning range was achieved at higher temperature, the mounting was performed in a manner to increase the thermal impedance R_θ, rather than decrease it.

4.6 TED DEVICE EVALUATION

The individual TED devices were characterized in detail. DC screening of the individual devices was started early in the TED fabrication process. The device is characterized as soon as the mesa etch step is complete. The initial measurement of the devices (I-V) cathode-anode current-voltage characteristics serve as a reference point. After each subsequent critical step in the process. The I-V characteristic is remeasured to ensure that the device has not degraded. In addition to providing a check on the fabrication process, the dc negative resistance characteristic must be present if the device is to operate properly at microwave frequencies. The presence of dc negative resistance does not ensure RF performance, but it eliminates defective devices early in the processing sequence. The TED's gate I-V characteristics also provide insight into the RF performance of the TED. The gate I-V characteristics are also monitored using the curve tracer and a scope camera to record the data. The measurement of gate I-V curves serves chiefly as an indication of the quality of the Schottky barrier contact. One of the key parameters of interest when TED's are being evaluated is gate triggering sensitivity. The gate I-V curves are not very informative in this regard. However, an indication of triggering sensitivity is gained by monitoring the cathode-anode I-V curve while varying the gate bias. Given two TED's which are physically the same, the device whose peak current is depressed further for a given change in gate bias will have the better trigger sensitivity. Additionally, the slope of the I-V characteristics in the high field region gives an indication of the trigger sensitivity. Flat slopes result on devices with poor trigger sensitivity.

Figure 4-10 shows a typical TED I-V characteristic. The negative resistance region of the characteristic can be clearly seen, the family of curves is generated by varying the gate voltage.

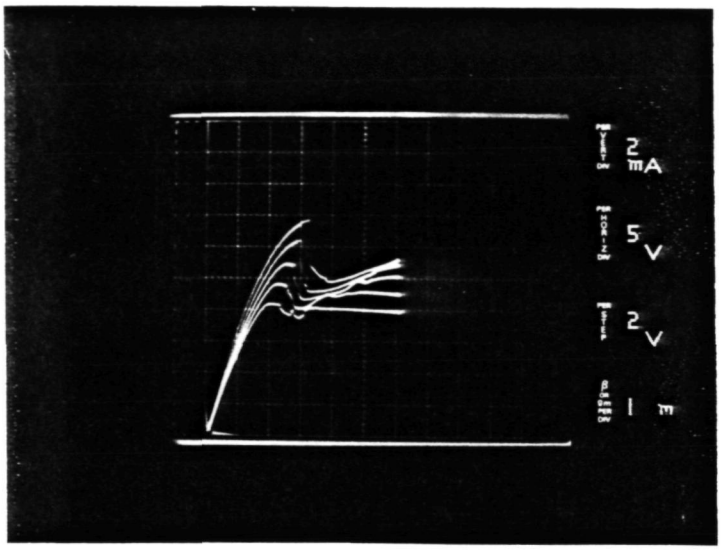

Figure 4-10. Typical TED I-V Characteristics

After completion of fabrication and DC evaluation, the TED devices were mounted in an RF evaluation test fixture. The RF evaluation fixture allows 50 ohm microstrip transmission lines to be connected to the TED's gate and anode. After the TED's are mounted in the RF test fixture, their RF characteristics could be evaluated in detail. The TED's were designed to operate at 2.14 GHz; however, the actual operating frequencies were somewhat high, typically in the 2.1 to 2.4 GHz range. The operating voltages were in the range of 25 to 45 volts on the anode and 0 to -4 volts on the gate. To achieve a 10 MHz locking range, an input power in the range of 0 to -18 dBm was required with a resulting output power in the range of -10 to -20 dBm. Figure 4-11 shows the locking bandwidths versus temperature and input power for a typical TED in a divider circuit. This figure clearly indicates a wider locking range at the higher operating temperature, a phenomenon typical of all the TED's measured. This characteristic appears to be related to a decrease in mobility in the GaAs at higher temperatures.

The decrease in mobility apparently reduces the triggering threshold of the device producing higher triggering sensitivity and wider band operation. A plot of this frequency variation with temperature is shown in Figure 4-12. Two sets of bias conditions are plotted. The TED's were

maintained at a constant operating frequency over a -23^{o} to $+65^{o}$F temperature range by adjusting the gate bias voltage. A plot of the required gate voltage for constant frequency operation for a typical TED is shown in Figure 4-13. The gate bias voltage could be used to temperature compensate the TED if the appropriate voltage-temperature characteristic was generated. The problem with this technique can be seen in Figure 4-11. The frequency of operation can be maintained using the gate bias but as the temperature decreases, the locking range also decreases.

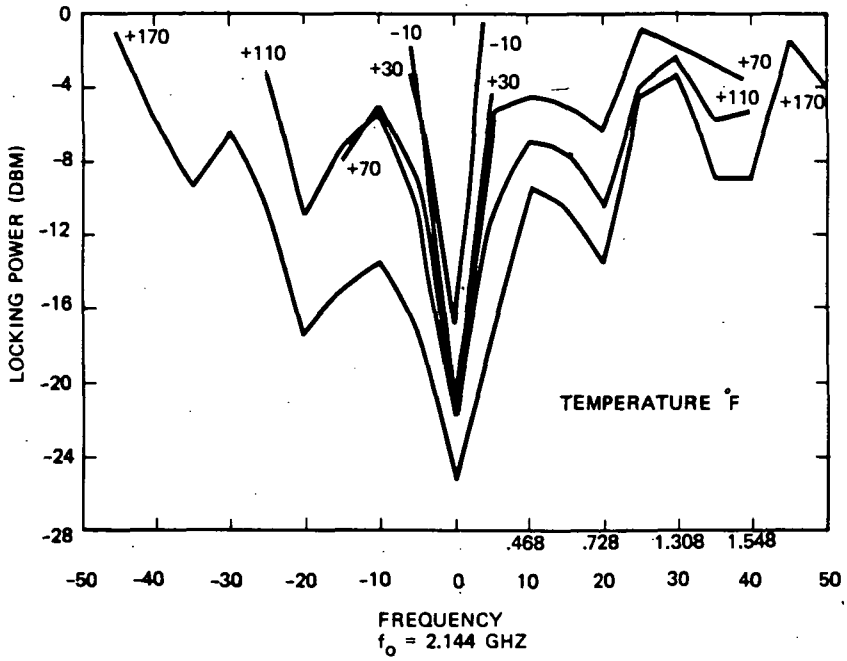

Figure 4-11. Locking Bandwidth versus Temperature and Input Power

4.7 TED TEMPERATURE COMPENSATION

Two general TED temperature compensation techniques were considered. The TED's operating frequency can be stabilized by adjusting the bias voltages as the temperature changes. This approach, however, has two major problems. The required bias voltages are extremely nonlinear and are unpredictable. Generating the temperature compensating bias voltage would require a complex circuitry which would have to be tailored to each individual TED. The bias compensation approach also has the problem of decreased locking bandwidth at lower temperatures. The bandwidth shrinkage phenomenon can be easily seen in the bandwidth versus temperature plot of Figure 4-11.

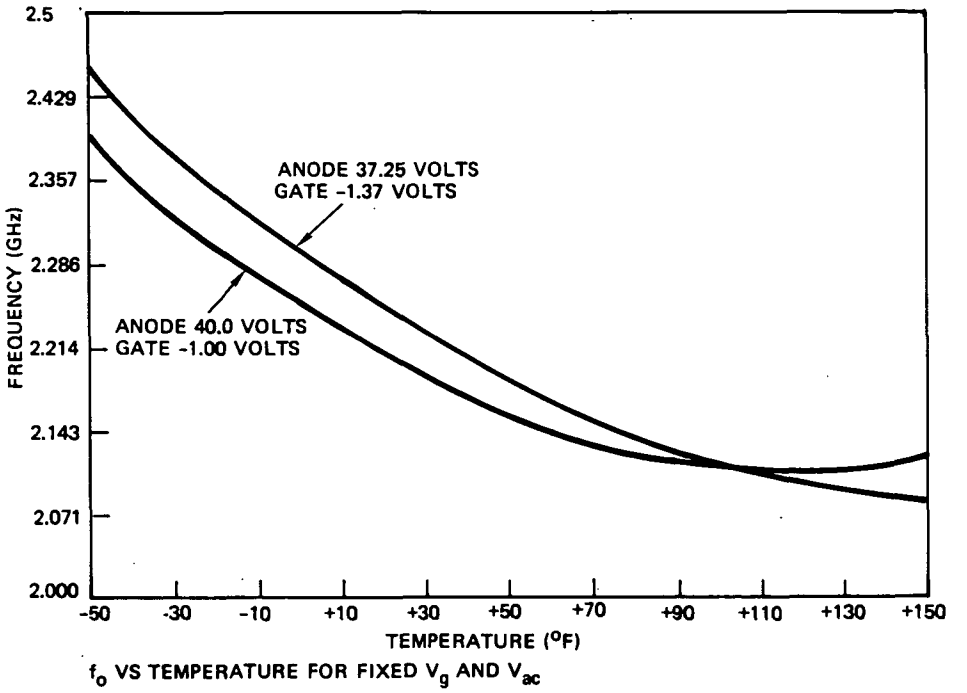

Figure 4-12. f_o versus Temperature

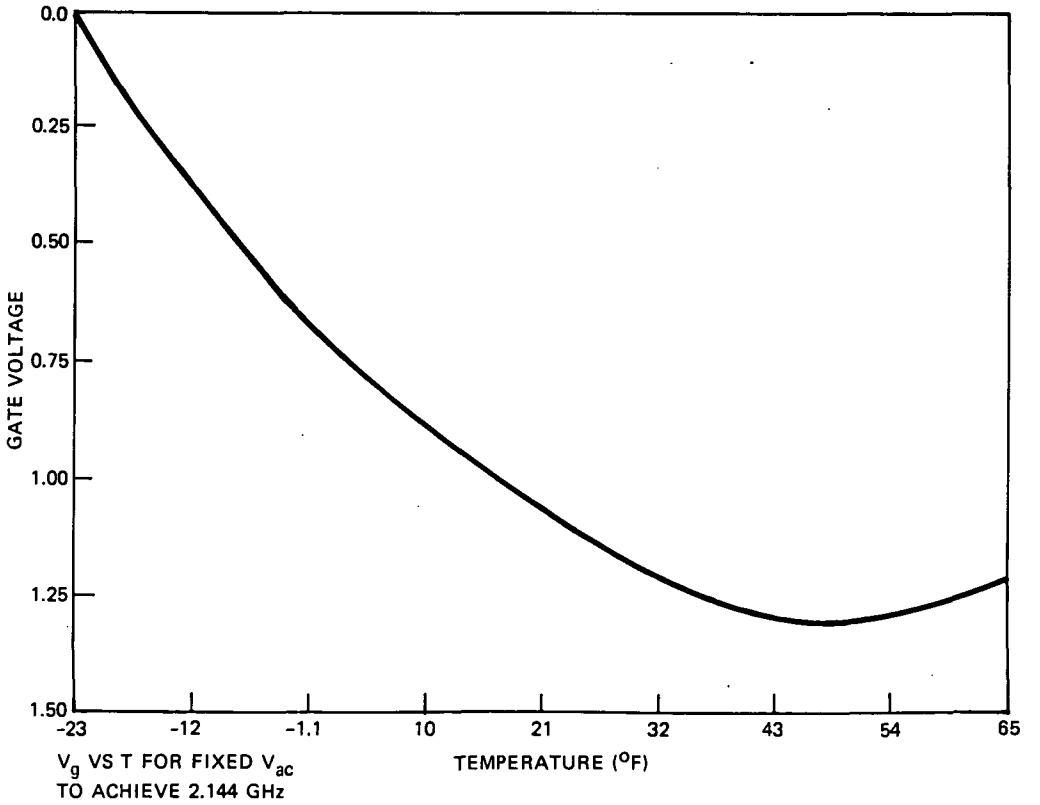

Figure 4-13. Gate Voltage Necessary to Maintain Constant Frequency versus Temperature

The second technique for extending the TED divider's operating range is to maintain the TED at a constant temperature. The TED temperature is maintained slightly above the highest operating temperature by externally heating the device as the operating temperature is reduced. The TED temperature-compensating circuit is designed to maintain the temperature at a fixed level at the high end of the circuits operating temperature range. To maintain a constant temperature, the TED device was mounted on a heating element. When the TED divider circuit's operating temperature is lower than the maximum limit, power is supplied to the heating element to maintain the temperature at a constant level. To control the temperature of the TED very precisely, a feedback type temperature regulator circuit was used. A temperature sensitive resistor was mounted with the TED to provide a feedback signal to the regulator circuit.

4.8 TEMPERATURE COMPENSATED TED MOUNTING ANALYSIS

An analysis is given of the thermal properties of the 2.144 GHz TED and the mounting materials. This thermal analysis is designed to determine the mounting media to be used to enhance external heating for broad band tuning of the TED's.

The configuration of a 10 x 5 mil TED device on a 15 mil cube of GaAs (Figure 4-14) mounted with 1 mil of conductive epoxy on a very large 250 mil gold plated kovar carrier is shown in Figure 4-15.

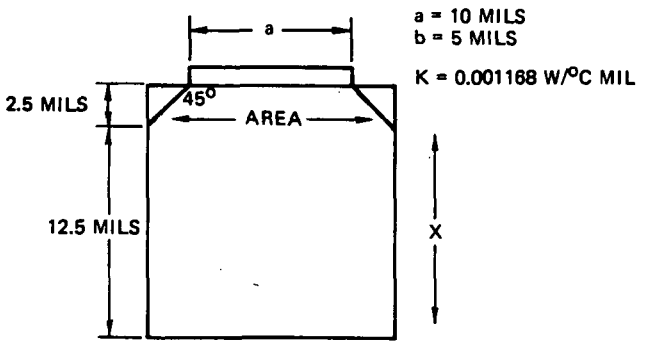

Figure 4-14. TED Thermal Model

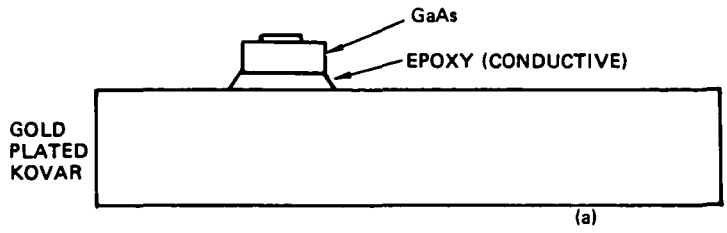

Figure 4-15. Epoxy Mounted TED Thermal Model

Neglecting radiation, the heat will flow from the device to the carrier. The heat flow path may be considered to be a network of thermal resistances. Since the thermal resistivity of air is very large compared to the resistivity of the other possible heat flow paths, radiation will be neglected.

Figure 4-16 shows a schematic representation of the basic thermal resistance network under consideration. Since this is a series network it is permissible to evaluate each component separately.

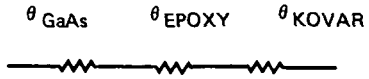

Figure 4-16. Basic TED Mounting Thermal Equivalent Network

$$\theta_{GaAs} = \frac{1}{K}\int_{0}^{2.5} \frac{dx}{Area(x)} + \frac{12.5}{KArea(x)}\Bigg|_{2.5}^{15.0}$$

$$\theta_{GaAs} = \frac{1}{2K(a-b)}\left[\ell n \; 2\left(\frac{(2\ x+b)}{(2\ x+A)}\right)\right]\Bigg|_{0}^{2.5} + \frac{x}{K(15\ mil)^2}\Bigg|_{2.5}^{15.0}$$

$$= 24.57^{o}C/w + 47.56^{o}C/w$$

$$\theta_{GaAs} = 72.13^{o}C/w$$

Similarly, for 1 mil of conductive epoxy with $K = 4 \times 10^{-5}$ w/°C mil

$$\theta_{epoxy} = 98^{\circ}C/w$$

and for 250 mils of kovar

$$\theta_{kovar} = 83.66^{\circ}C/w$$

However, we will consider the kovar due to its size to be at the ambient temperature.

The total thermal impedance for the system in Figure 4-17 is $\theta_{total} = 170^{\circ}C/w$. If a 10 mil thick alumina substrate is placed under the chip, a system like that shown in Figure 4-17 is achieved.

The contribution of the alumina will be an additional $\theta_{alumina} = 17.86^{\circ}C/w$ and the 1 mil of conductive epoxy between the alumina and the gold plated kovar is an additional $\theta_{epoxy\ 2} = 17.32^{\circ}C/w$. Thus, for the system in Figure 4-17 $\theta_{total} = 205.18^{\circ}C/w$.

One problem with this system is that it is very difficult to control the thickness of the epoxy. This is not too critical for the layer between the alumina and the kovar, but is critical between the device and the alumina. Because it is important to be able to predict θ_{total}, a more repeatable system is required. A system is needed where the bonding agent is repeatable and the substrate controls the device heating.

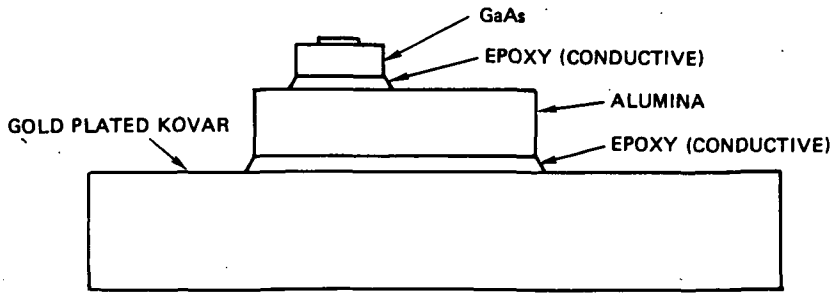

Figure 4-17. TED Mounted on Alumina Substrate

In Figure 4-18, we have replaced the epoxy with a AuGe eutectic alloy. This thickness is very controllable and has a very low thermal resistivity. Small thickness variations have little effect on total θ. The thermal conductivity, K, for the eutectic is around 5.5×10^{-3} w/^{o}C mil. Because the epoxy, which had a high thermal resistivity, is not used, another high resistivity material with a reliable thickness is needed. Glass has been chosen since it has a K of 4×10^{-5} w/^{o}C mil.

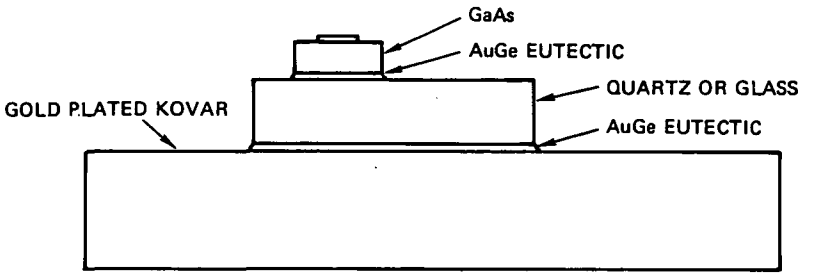

Figure 4-18. Controlled Thermal Resistance TED Mounting

When compared to the other thermal resistances involved, θeutectic = 0.713^{o}C/watt, $\theta_{\text{eutectic 2}}$ = 0.14^{o}C/watt, which is negligible and can be neglected.

Table 4-2 shows the θ for glass and the total θ, for various thickness of the glass substrates, and ΔT_j for 120 mW.

Table 4-2. Glass Thermal Characteristics

(Inch)	θ_{glass} (^{o}C/W)	θ_{total} (^{o}C/W)	ΔT_j (^{o}C)
0.005	333	405	48.6
0.010	476	548.8	65.76
0.020	606	678.8	81.36
0.025	641	713.8	85.66
0.030	666	738.8	88.56
0.045	714	786.8	94.32
0.060	740	812.8	97.54

Another possible method of raising the junction temperature is to create an artificial ambient temperature by localized heating of the chip. If a resistor was placed on a thickly Au plated glass substrate, the surface could be uniformly heated. In Table 4-3, θ_{glass} is shown for various thicknesses, assuming a 50 mil square surface. The ΔT_j is also shown for assuming 500 mW dissipation by the resistor and 120 mW input power to the TED.

Table 4-3. TED Mounting Thermal Characteristics

(Inch)	θglass ($^oC/w$)	ΔT_j at 500 $mW_{(resist.)}$ + 120 mW(device) (^oC)
0.005	50	33.74
0.010	100	58.74
0.020	200	108.74
0.025	250	133.74
0.030	300	158.74
0.045	450	233.74
0.060	600	308.74

4.9 TED TEMPERATURE COMPENSATION CIRCUIT DETAILED DESIGN

The TED temperature compensation circuit consists of the temperature regulator circuit and, in addition to the TED, a mounting structure made up of a heating element, temperature sensor, and a thermal insulator. The temperature regulator circuit shown in Figure 4-19 uses an LM108 operational amplifier as a dc comparator. The LM108 compares the voltage developed across a temperature sensitive resistor, sensistor, with a fixed reference voltage. The amplified error voltage output of the LM108 controls the input of the heater driver transistor, a 2N2907. The heater driver transistor controls the amount of power dissipated in the TED heating element, a 150 ohm chip resistor. The complete regulator circuit was built using discrete components assembled on the duroid interconnect board in the TED divider assembly housing.

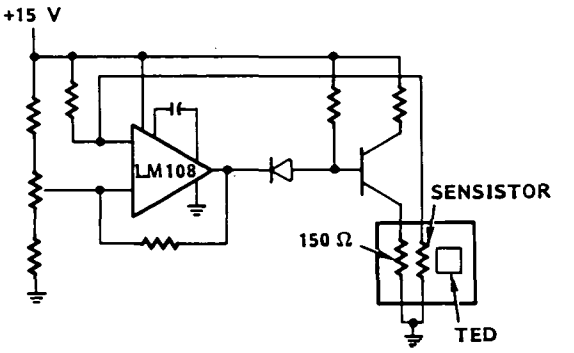

Figure 4-19. Temperature Regulator Circuit Schematic Diagram

The TED mounting structure is the key element in this temperature compensation technique. Figure 4-20 is a pictorial diagram of the TED mounting configuration; Figure 4-21 is a photo of a TED and the temperature compensating mounting structure. The TED and temperature sensing resistor (sensistor) are mounted on top of a 150 ohm resistor serving as a heating element. The TED gate, cathode, and anode leads are connected to gold bond pads which are also mounted on top of the 150 ohm resistor. These bond pads are the result of early experiments with the TED temperature compensation mounting structure. Without the bond pads, the TED experienced temperature differentials in the wire bonding areas due to thermal conditions through the connecting wires. The bond pads are maintained at the same temperature as the TED, therefore heat conduction through the TED's bond wires is eliminated.

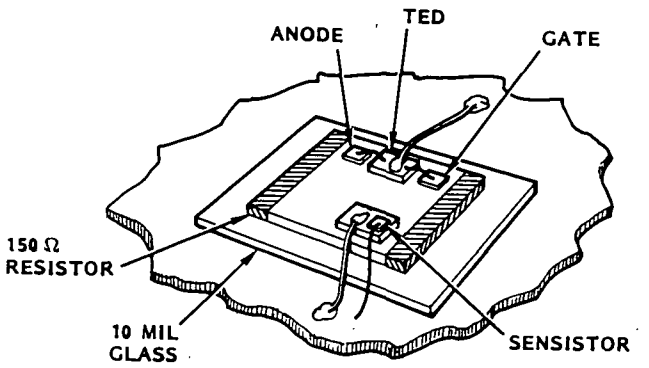

Figure 4-20. Temperature TED Mounting Structure

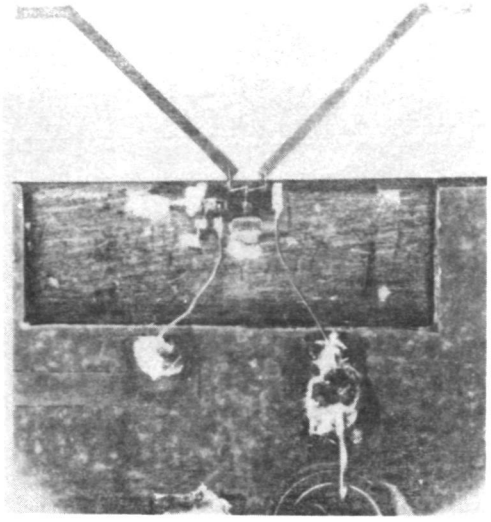

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Figure 4-21. 2.144 GHZ TED

The 150 ohm resistor heating element is mounted on a 10 mil glass plate. The glass plate provides a known amount of thermal resistance between the TED and the heatsink. The 10 mil glass was used because the thermal resistance is such that the heat generated by the TED at high temperature can be dissipated, while providing a thermal resistance between the heating element and the heatsink. The added thermal resistance reduces the amount of power required to heat the TED during low temperature operation.

4.10 TEMPERATURE COMPENSATED TED DATA SUMMARY

The temperature-compensated TED divider was tested over a 0 to 120^{o}F temperature range. A usable output locking range in excess of 8 MHz was achieved over the entire temperature range. The TED divider was operated with a 15 GHz input signal at a power level of 0 dBm. The locking range data, shown in Figure 4-22, indicates that the TED frequency shifts approximately 3 MHz over the full 0 to 120^{o}F temperature range. A typical TED would have a frequency shift in excess of 200 MHz over this temperature range without the use of temperature compensation. The temperature compensation circuit reduces the frequency drift to only 1.5 percent of that of an uncompensated TED. The dc power dissipated in the 150 ohm TED heater resistor varies from 1.215 watts at 0^{o}F to 80 mW at 120^{o}F.

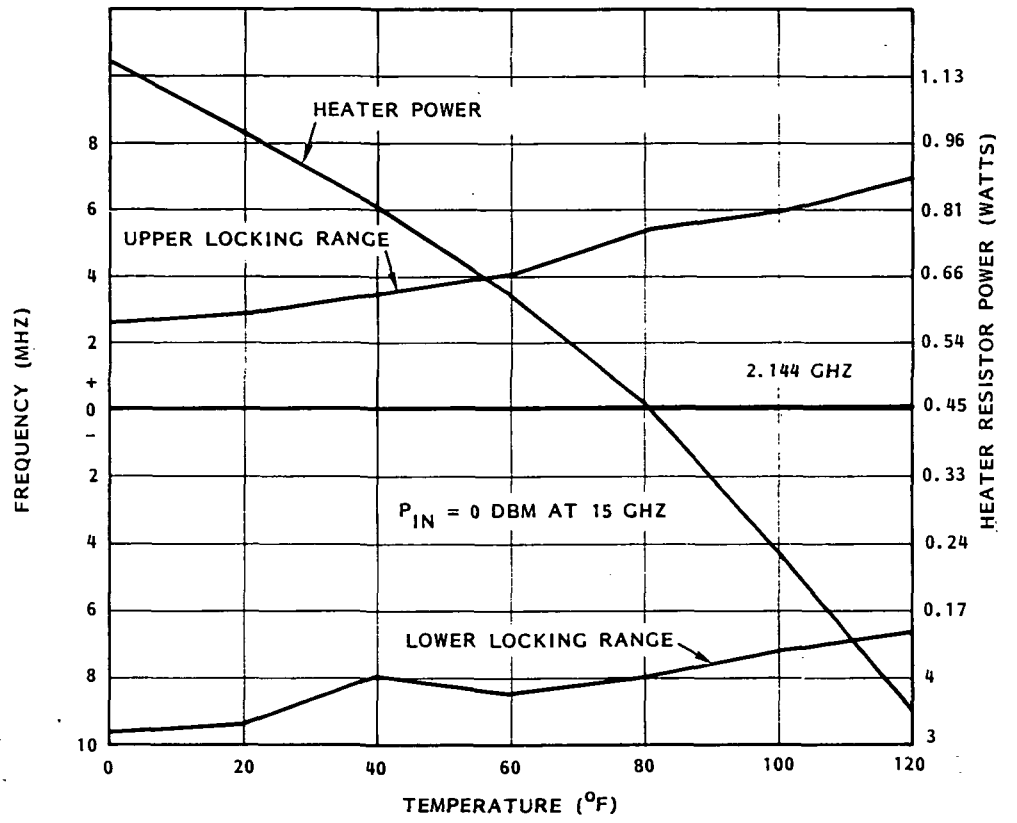

Figure 4-22. TED Divider Locking Range

5. KU-BAND SOURCE

Phaselocked fundamental microwave oscillators have several features which make them ideal candidates for high performance microwave signal source applications. The Ku-band sources fabricated for this program used a 15 GHz FET VCO phaselocked to a 2.14 GHz reference source using both divider and multiplier techniques. The phaselocking technique eliminates the need for the high degree of filtering required by a multiplier source.

5.1 OBJECTIVES

The objective of this task was to design and fabricate high performance Ku-band phaselocked signal sources. Two types of phaselocked Ku-band sources were constructed; one using a multiplied reference signal to phaselock the Ku-band oscillator, the other using a divided output signal for phaselocking. The two Ku-band sources were fabricated as part of two programs composed of the following tasks:

Phase 1:
- Design and fabrication of a multiplier type phaselocked Ku-band frequency source
- Characterize the multiplier Ku-band source.

Phase 2:
- Design and fabricate a divider type phaselocked Ku-band frequency source
- Characterize the divider type Ku-band source.

5.2 SOURCE CONFIGURATION STUDY

A detailed configuration study was performed in order to objectively compare the potential performance and risks involved with the two possible circuit approaches. The results of this study determined the baseline design approach to be used on the Ku-band source.

The two possible circuit approaches were either frequency multiplication or division to achieve phase comparison between the 2 GHz SAW oscillator and the 15 GHz FET VCO. The multiplier approach multiplies the lower frequency reference to the output frequency, while the divider technique divides the output frequency to the reference frequency.

The two techniques were compared on the basis of both physical and electrical characteristics. The particular parameters considered were size, weight, power, complexity, temperature performance, and phase noise.

5.2.1 X7 Multiplier Approach

A block diagram of the multiplier type 15 GHz source is shown in Figure 5-1. The X7 multiplier source multiplies the 2.2 GHz reference signal by seven to generate a 15 GHz reference signal. The phase comparison between the 15 GHz multiplied reference signal and the 15 GHz VCO signal is accomplished with a 15 GHz phase detector.

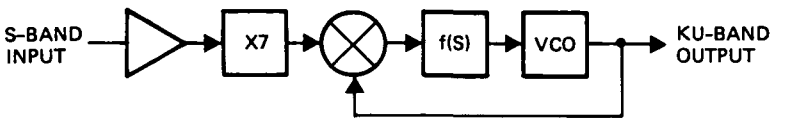

Figure 5-1. Multiplier Type Ku-Band Source Block Diagram

The X7 multiplier requires a fairly high input level, 17 dBm at 2.2 GHz. An amplifier is required to raise the SAW oscillator's output level to the 17 dBm level. The input amplifier in the actual hardware has been designed into the SAW oscillator. The 15 GHz output signal at a 5 dBm level is used to drive the reference input port of the 15 GHz phase detector. The signal input from the phase detector is obtained from a power divider on the output of the 15 GHz FET voltage controlled oscillator (VCO). The phase detector output is conditioned by the loop filter, F(s), and routed to the VCO frequency control input. The 15 GHz FET VCO is therefore phaselocked to the 2.144 GHz input signal.

5.2.2 TED Divider Approach

A block diagram of the TED divider type 15 GHz source is shown in Figure 5-2. The TED divider circuit generates a 2.2 GHz signal which is phase-coherent with the 15 GHz VCO signal. The phase comparison between the 2.2 GHz reference signal is accomplished with a 2 GHz phase detector.

A 15 GHz signal at approximately 0 dBm is coupled from the VCO output to the input of the TED divider circuit. The TED divider has an output of approximately -10 dBm at 2.2 GHz. The TED output level is amplified to +7 dBm to drive the signal input of the S-band phase detector. The phase

detector compares the 2.2 GHz signal with the 2.2 GHz reference input. The phase error output voltage from this phase detector is conditioned by the loop filter and routed to the 15 GHz FET VCO frequency control input. The FET VCO is therefore phaselocked to the 2.2 GHz reference signal input.

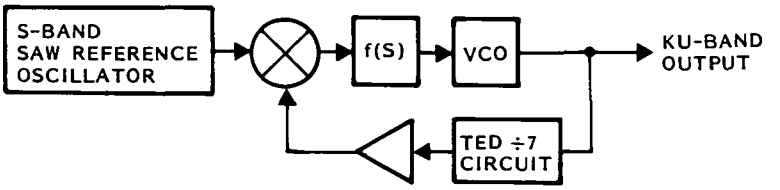

Figure 5-2. Divide Type Ku-Band Source Block Diagram

5.3 15 GHz MULTIPLIER SOURCE DESIGN CONCEPT

The 15 GHz multiplier source was implemented by interconnecting individually housed functional circuit modules with coaxial cable. The complete 15 GHz source consists of five interconnected modules. The five functional circuit modules are the 2.14 GHz temperature compensated SAW oscillator, the X7 multiplier, the 15 GHz phase detector, the 15 GHz FET VCO, and the loop filter circuit. The 2.14 GHz temperature compensated SAW is a 2.7 x 3.7 x 1.9 inch aluminum housing with an SMA output connector. The SAW oscillator is described in detail in Section 3.3 of this report.

The 17 dBm output of the 2.14 GHz SAW oscillator drives the input of the X7 multiplier. The X7 multiplier uses a varactor diode as the nonlinear multiplier element. The multiplier is fabricated on a duroid circuit board using microstrip lines as circuit elements. The multiplier provides a 5 dBm output signal at 15 GHz which drives the reference input of the 15 GHz phase detector.

The quadrature phase detector has two phase error outputs which are 90^{o} out of phase with each other. One output is used as the phase error output, the other output is used as a coherent amplitude detector (CAD) to sense a phaselocked condition. The phase detector has been fabricated on an alumina substrate mounted in a 1.5 x 0.6 x 0.3 inch housing. The signal input of the phase detector is driven by a 2.5 dBm signal from the 15 GHz FET VCO.

The FET VCO is a modular type design made up of individual amplifier circuits and a cavity resonator interconnected in a 2.3 x 1.8 x 1.1 inch aluminum housing. The FET VCO's individual functional circuit elements are mounted on carriers which are mounted in the VCO housing. The individual circuits are interconnected with microstrip transmission lines on duroid boards. The FET VCO provides a power-divided 5.5 dBm 15 GHz output signal. The power-divided FET VCO output drives the signal input of the phase detector and provides the source's output signal.

The final Ku-band source circuit module is the loop filter and acquisition circuit. The loop filter was implemented using an operational amplifier as an active lowpass filter. The loop filter and the acquisition circuit were assembled using discrete components assembled on a printed circuit board. The complete assembly is housed in a 5.0 x 2.0 x 1.5 inch aluminum housing.

The complete 15 GHz source was assembled on two 4.8 x 10.5 inch aluminum plates. The two plates were stacked with all the RF circuits mounted on the top plate and the loop filter mounted on the bottom plate.

5.4 MULTIPLIER SOURCE DETAILED CIRCUIT DESIGN

A detailed block diagram of the multiplier type 15 GHz source is shown in Figure 5-3. The multiplier source is made up of five functional circuit modules which contains the majority of the circuitry. The interconnecting coaxial cables, the dc power connections, and the power divider are the only items not contained within the circuit module.

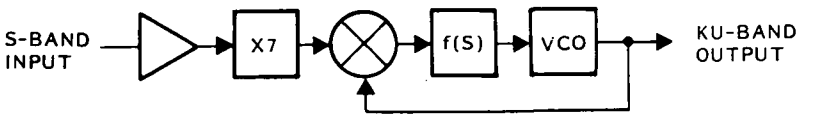

Figure 5-3. Multiplier Type 15 GHz Source Diagram

5.4.1 FET VCO

The FET VCO was configured using a circuit similar to that of the lower frequency SAW oscillators; that is, a high-Q frequency-determining element in series with a feedback amplifier. This approach takes advantage of the mature FET amplifier circuit technology existing for frequencies up to 18 GHz. In addition, the characteristics of feedback oscillators are well understood, and the performance of any given oscillator can be accurately predicted based on the performance of the individual elements within the oscillator. A stable, high-Q hybrid MIC-compatible resonator was realized using a very thin cylindrical cavity, shown in Figure 5-4.

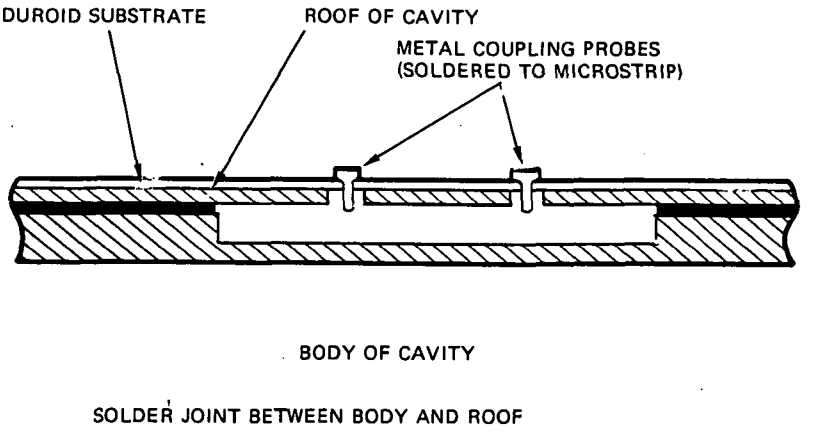

Figure 5-4. Thin Cavity Resonator Cross Section

At 15 GHz the cavity diameter is 0.6 inch. Cavity Q is directly proportional to the height of the cavity. Theoretical unloaded Q for a gold-plated, air-dielectric cavity only 0.050 inch deep is 1500, which is more than sufficient for the oscillator application. The theoretical expressions for Q and resonant frequency for the cylindrical cavity are given below:

$$f = \frac{2\pi\alpha c}{\alpha_1}$$

$$Q = \frac{\alpha_1 N}{R1+\frac{a}{d}}$$

where:

α_1 = first zero of $J_0(x)$

N = μ/G = 377 for air dielectric

a = cavity radius

d = cavity height

c = speed of light

Coupling in and out of the cavity is by capacitive probes positioned along a diagonal of the cavity approximately one-half radius from the center. The degree of coupling to the cavity is controlled by adjusting the probe depth. Cavity resonant frequency is controlled by a third grounded probe in the top of the cavity. The cavity is designed to have a nominal frequency 5 percent above the desired operating frequency and is then loaded with the probe to lower its frequency. Using this technique, a single cavity has been tuned from 16 down to 12 GHz. The swept response of the cavity when tuned to 15.0 GHz is shown in Figure 5-5. The insertion loss was 6 dB with a 3-dB bandwidth of 27 MHz.

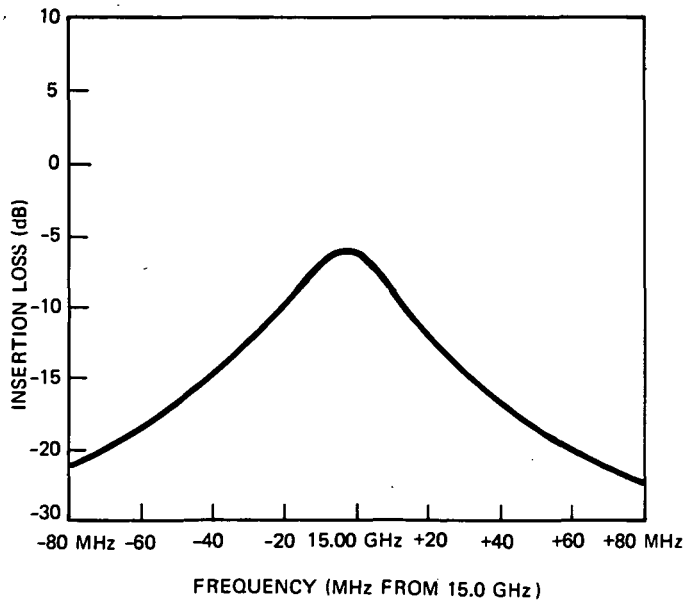

Figure 5-5. Cavity Resonator Amplitude Response

The thin cavity structure is ideally suited for the hybrid MIC FET oscillator. The cavity is easily machined into the floor of the oscillator flatpack under the microstrip circuitry above it. The result is the extremely efficient integration of an electromechanical cavity within a hybrid circuit.

The complete block diagram for the 15 GHz FET oscillator is shown in Figure 5-6. The circuit consists of a three-stage FET amplifier, varactor-tuned cavity resonator, and a 3 dB power splitter. As shown in Figure 5-7, the complete breadboard oscillator is assembled in a 2 x 1.6 x 1 inch housing.

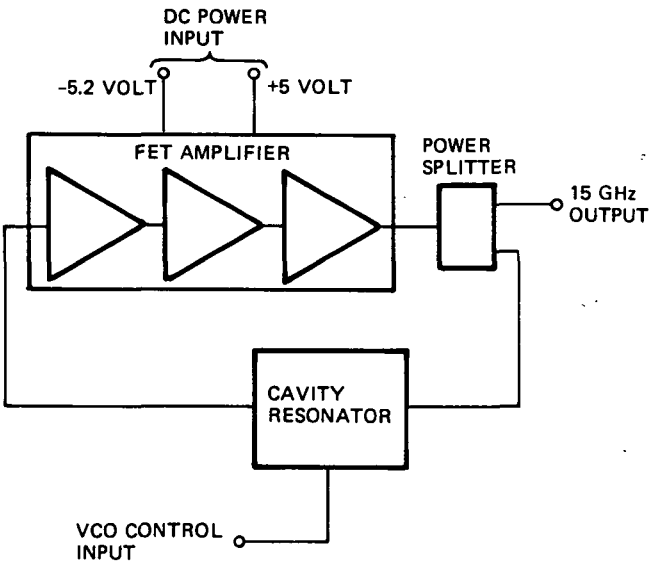

Figure 5-6. FET VCO Block Diagram

The critical oscillator parameter is phase noise. The measured performance of the oscillator is shown in Figure 5-8. In addition to the phase noise measurements, the oscillator was extensively characterized; the performance of the oscillator is summarized in Table 5-1. The current oscillator design uses a Kovar cavity which results in a temperature stability of $\pm$0.03 percent. For the breadboard oscillator, output power varied <0.2 dB over 0 to +120^{o}F temperature range and all spurious were <-60 dBc. As a VCO, the FET oscillator has a tuning range of $\pm$5 MHz.

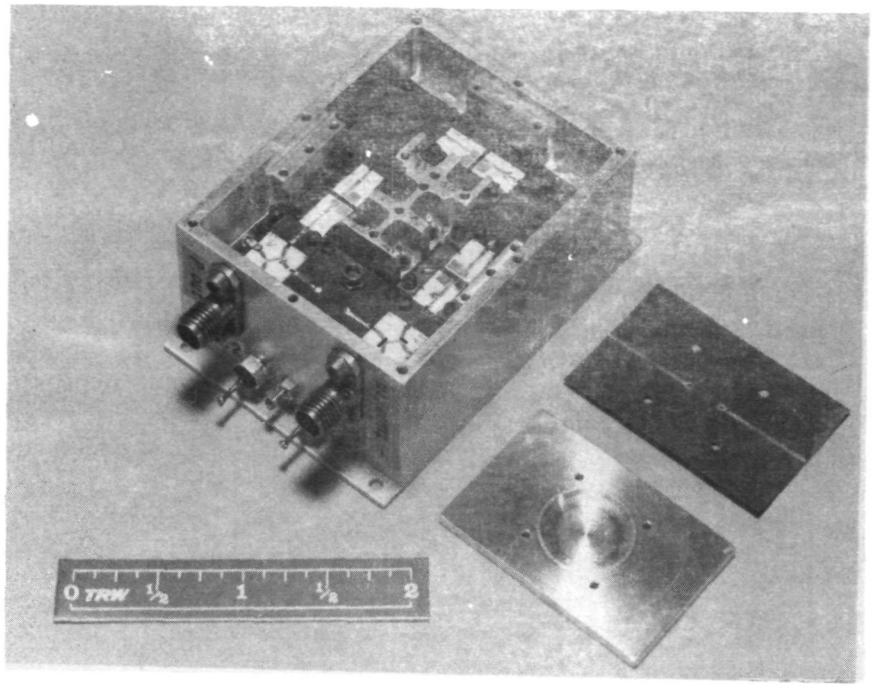

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Figure 5-7. 15 GHz Oscillator

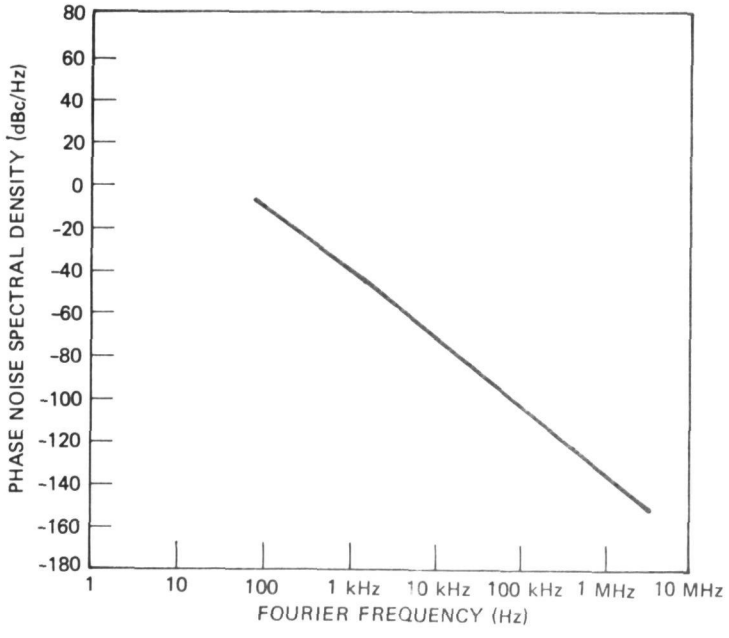

Figure 5-8. FET VCO Phase Noise

Table 5-1. Ku-Band FET VCO Performance Summary

Parameter	Performance
Frequency	15.0 GHz
Frequency Stability	±0.03%
0 to +120°F	
Output Power	+3.5 dBm
Power Stability	±0.2 dBm
0 to +120°F	
Phase Noise	
1 kHz	-40 dBc/Hz
10 kHz	-70 dBc/Hz
100 kHz	-100 dBc/Hz
1 MHz	-130 dBc/Hz
VCO Range	±5 MHz
Spurious	<-60 dBc
Resonator Q	>600
DC Power	175 mW

5.4.2 X7 Multiplier

The microstrip multiplier is an extension of previously developed coaxial and waveguide designs. The circuit consists of a lowpass input matching network, a step-recovery diode, diode bias circuitry, and an output bandpass matching network, all fabricated using microstrip circuit elements (Figure 5-9).

The X7 multiplier was fabricated on a 1.0 x 2.3 inch duroid substrate. As shown in Figure 5-10, the complete X7 multiplier is assembled on a 1 x 2.25 x 0.5 inch plate.

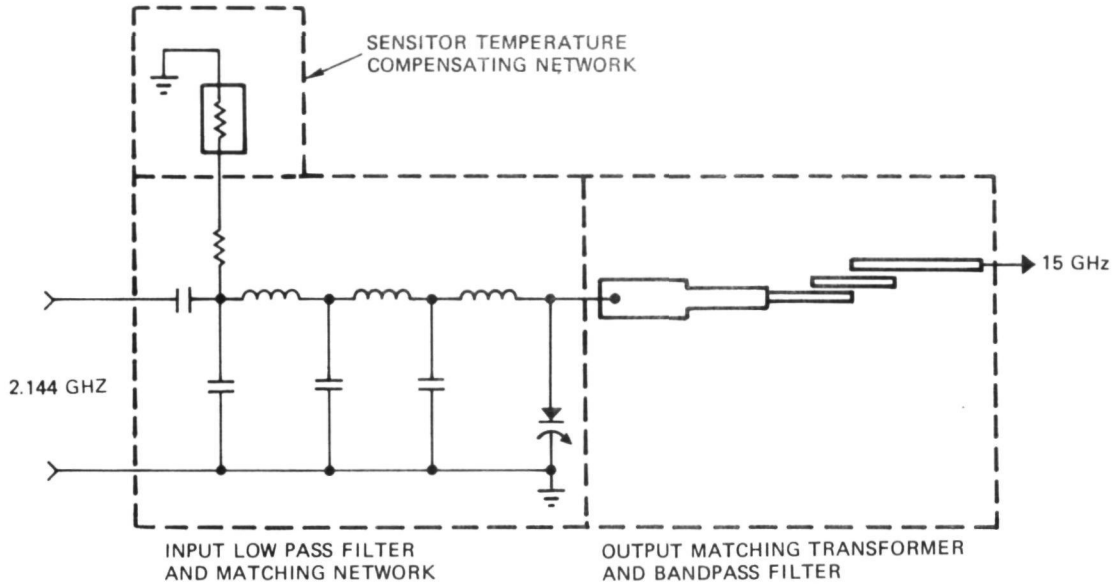

Figure 5-9. Schematic Diagram

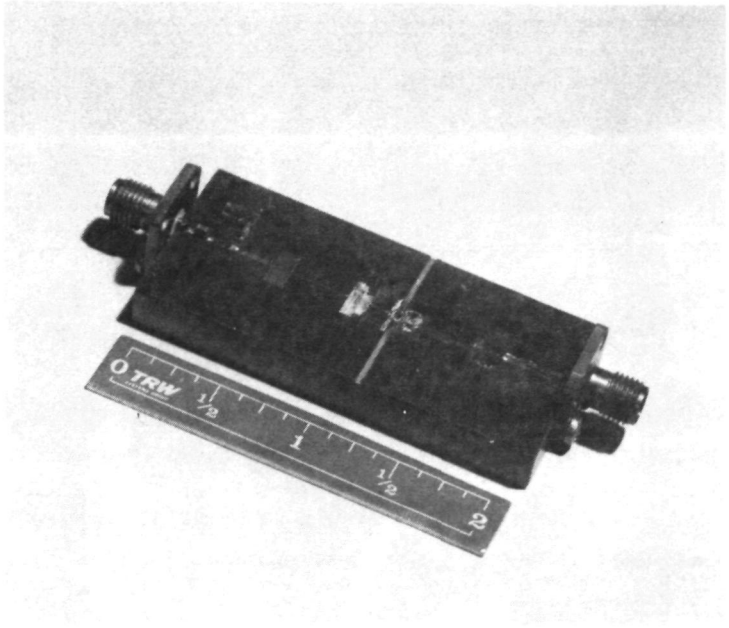

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Figure 5-10. 15 GHz X7 Microstrip Multiplier

The design goals for the X7 multiplier circuit are listed in Table 5-2. All of the values are based on an allocation of the Ku-band frequency performance requirements. Because the output of the multiplier does not serve as the final output of the source, but rather only as the reference input to the phase detector, the performance requirements are not stringent. Measured data for the multiplier is also shown in Table 5-2.

Table 5-2. X7 Multiplier Performance

Parameter	Design Goal	Breadboard Performance
Input Frequency	2.15 GHz	2.15 GHz
Input Power	+17 dBm	+17 dBm
Output Power	+5 dBm	+5 dBm
Output 3 dB Bandwidth	>±250 MHz	+300 MHz -400 MHz
Output Power Stability 0 to 100°F	<±1 dB	±0.5 dB
Spurious	<-20 dBc	-22 dBc

All performance goals were met or exceeded. As can be seen in Figure 5-11, the swept response of the multiplier is free of breakup or spurious responses over an output bandwidth of ±1 GHz. The multiplier output level of 5 dBm is achieved with a 17 dBm input level, and all spurs are greater than 20 dB below the input. To further confirm the performance of the multiplier, it was integrated with the 2.14-GHz SAW oscillator (previously described) and the pair characterized as a function of temperature. Over the range of 0 to 100°F, the multiplier output power varied <±0.25 dB, and the unit was free of breakup or spurious responses. A plot of the multiplier output, power versus temperature, is shown in Figure 5-12.

5.4.3 15 GHz Phase Detector

The MIC 15 GHz phase detector consists of a pair of mixers, 90° hybrid, in-phase power splitter and two lowpass filters (see Figure 5-13). The phase detector has two outputs: a phase error and a coherent amplitude. The coherent amplitude output is used to turn off the phaselocked

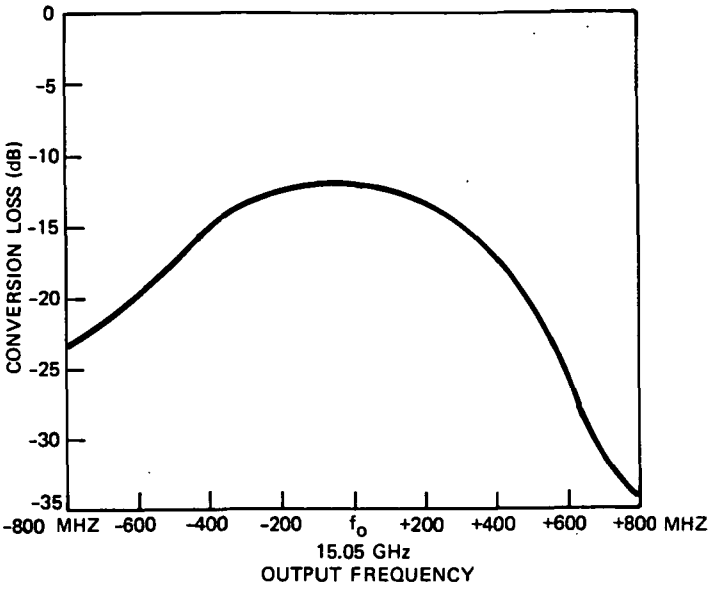

Figure 5-11. X7 Multiplier Swept Response

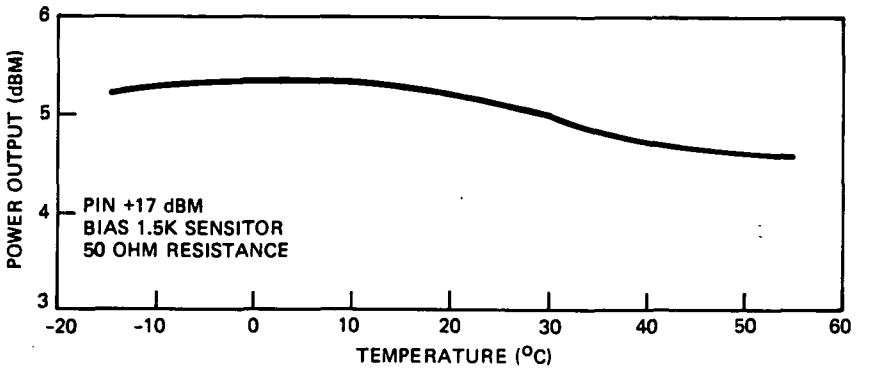

Figure 5-12. Multiplier Output Power versus Temperature

loop sweep circuits and as a telemetry lock indicator. The phase detector is configured using metal strip geometry circuitry on an alumina substrate structure and is formed by a pair of diodes mounted at the interface between a coplanar and slot transmission line. Two phase detectors, a 90^{o} phase hybrid and an in-phase power divider, are fabricated within the 0.6 x 1.5 x 0.3 inch phase detector housing shown in Figure 5-14. The phase detector operates over a bandwidth in excess of $\pm$200 MHz with input levels of approximately +5 dBm. The phase detector's sensitivity versus drive level characteristics are shown in Figure 5-15.

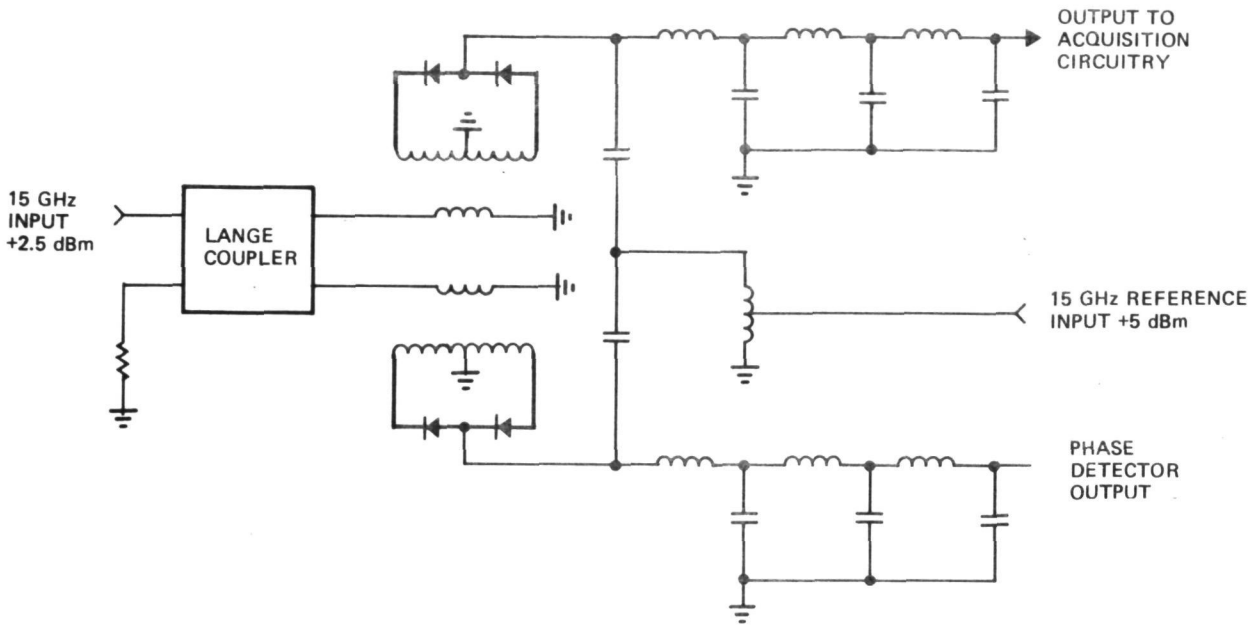

Figure 5-13. Schematic Diagram

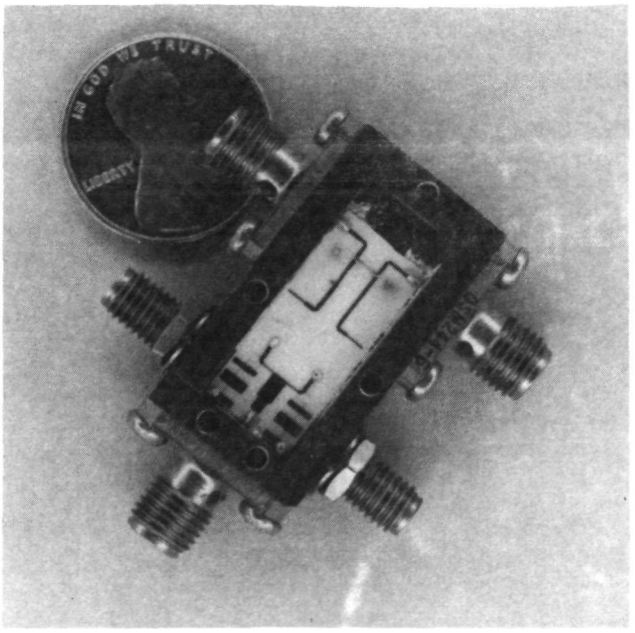

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Figure 5-14. 15 GHz Microstrip Phase Detector

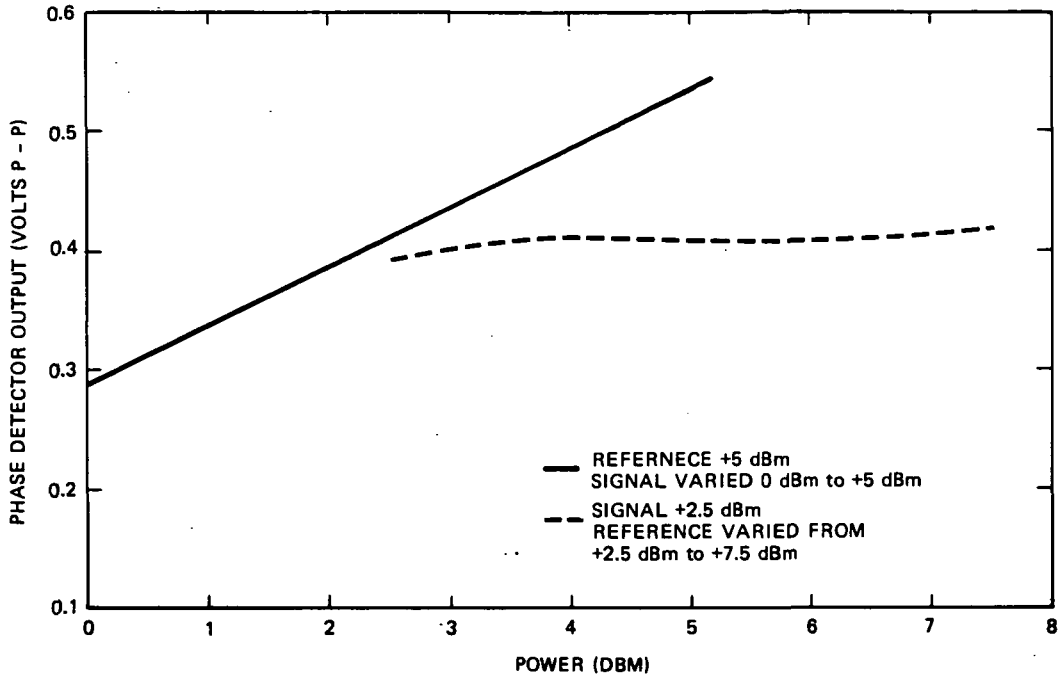

Figure 5-15. Phase Detector Sensitivity

5.4.4 Loop Filter

The loop filter contains three functional parts of the phaselocked loop system. Figure 5-16 is a functional block diagram of the circuitry contained in the 1.5 x 2.0 x 5.0 inch loop filter assembly.

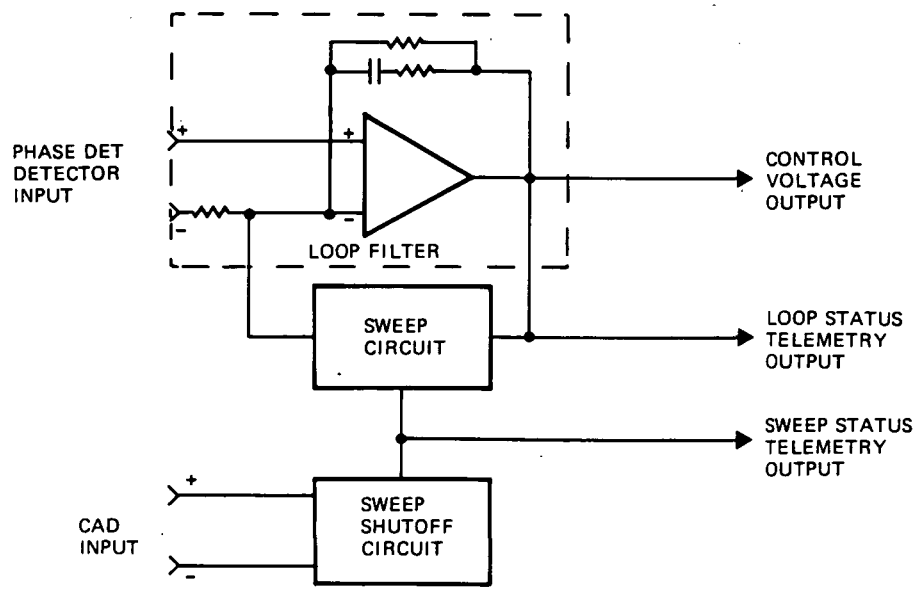

Figure 5-16. Loop Filter Functional Block Diagram

The primary function of the loop filter is to provide the phaselocked loop lowpass filter function. The loop filter uses an LM108 operational amplifier as the gain element in an active lowpass filter. In addition to the lowpass filter function, the loop filter circuit provides an acquisition sweep circuit and a sweep shutoff circuit.

The sweep circuit is a simple feedback circuit that turns the active lowpass loop filter into a triangle wave oscillator in the acquisition mode. The output of the LM108 active lowpass filter controls the input of a schmitt trigger circuit. The schmitt trigger's switch points are set at the sweep output voltage limits, 2 and 13 volts. The output of the schmitt trigger supplies an inphase offset current to the input of the active loop filter. The offset current causes the loop filter to act as an integrator and produces a ramp output voltage. When the ramp voltage reaches the schmitt trigger switch point the polarity of the offset current is reversed and the ramp reverses direction.

When the loop phase locks, the phase detector input cancels the sweep offset and the sweeping action stops. The coherent amplitude detector also senses a phaselocked condition and turns off the sweep circuit, thereby removing the loop stress caused by the sweep offset circuit. Figure 5-17 is a schematic diagram of the loop filter circuit.

5.5 MULTIPLIER SOURCE DATA SUMMARY

The performance of the complete Ku-band multiplier type frequency source is shown in Table 5-3. The Ku-band multiplier type source consists of the 15 GHz FET VCO which has been phaselocked to a 2.14 GHz temperature compensated SAW oscillator. The phaselock circuit multiplies the SAW oscillator's 2.14 GHz output to 15 GHz for phase comparison. The resulting Ku-band frequency source has come characteristics of each oscillator resulting in overall performance superior to either individual oscillator. Figure 5-18 summarizes the temperature characteristics of the phaselocked Ku-band source. The phase noise characteristics of the Ku-band source are shown in Figure 5-19. The bandwidth of the phaselocked loop is 20 kHz (see Figure 5-20), the transition from the reference oscillator phase noise to the FET VCO phase noise occurs at this frequency.

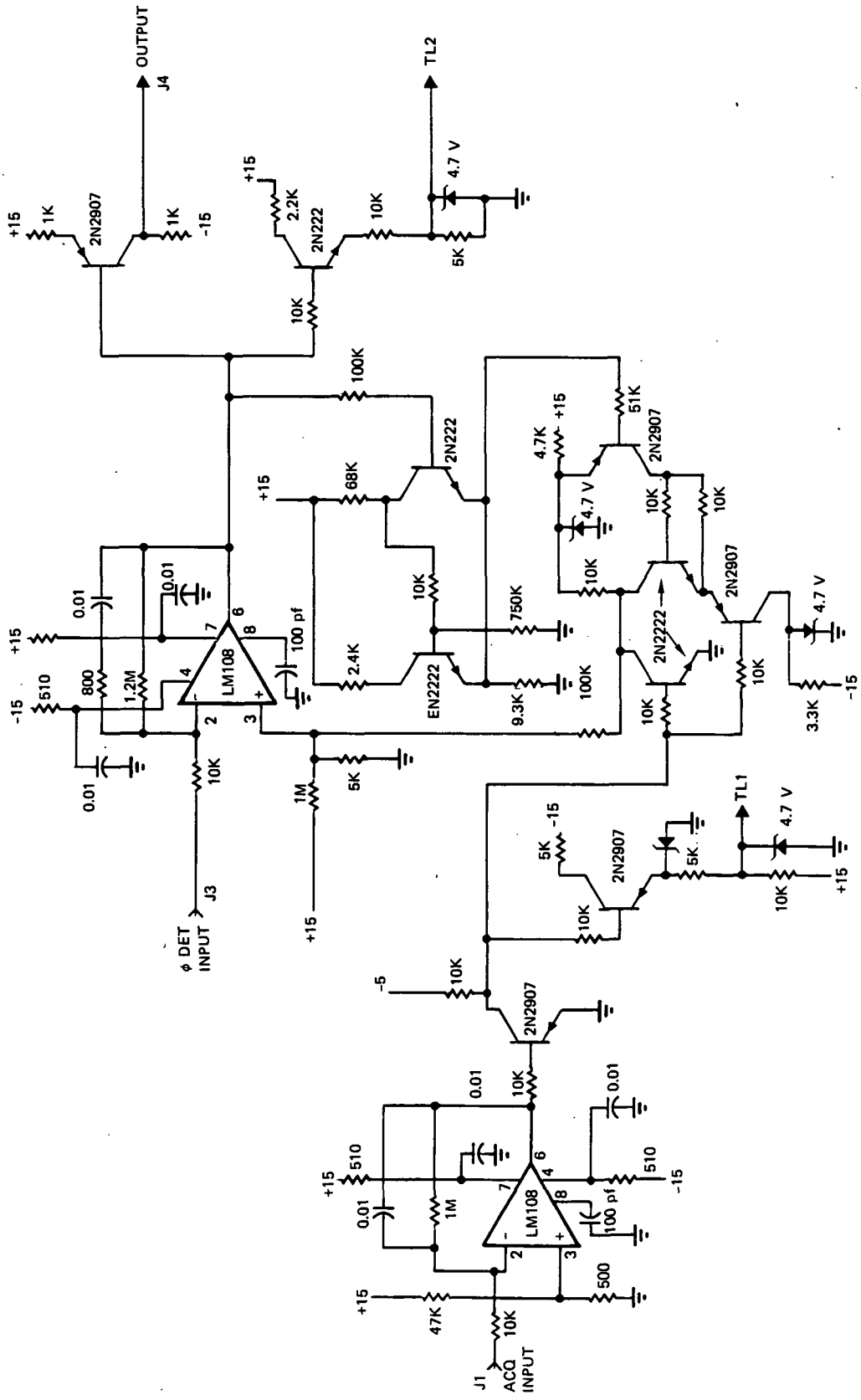

Figure 5-17. Loop Filter Schematic Diagram

Table 5-3. Ku-Band Multiplier Type Frequency Source Performance Summary

Parameter	Performance
Frequency	15.035 GHz
Temperature Stability	±0.023 percent (±3.36 MHz)
Phase Noise	
100	-24 dBc/Hz
1 kHz	-53 dBc/Hz
10 kHz	-69 dBc/Hz
100 kHz	-96 dBc/Hz
1 MHz	-132 dBc/Hz
Output Power	-2.5 dBm ±0.5 dB
DC Power	6.1 watts
Temperature Range	65°F to 118°F
Spurious (10 to 18 GHz)	<-60 dBc

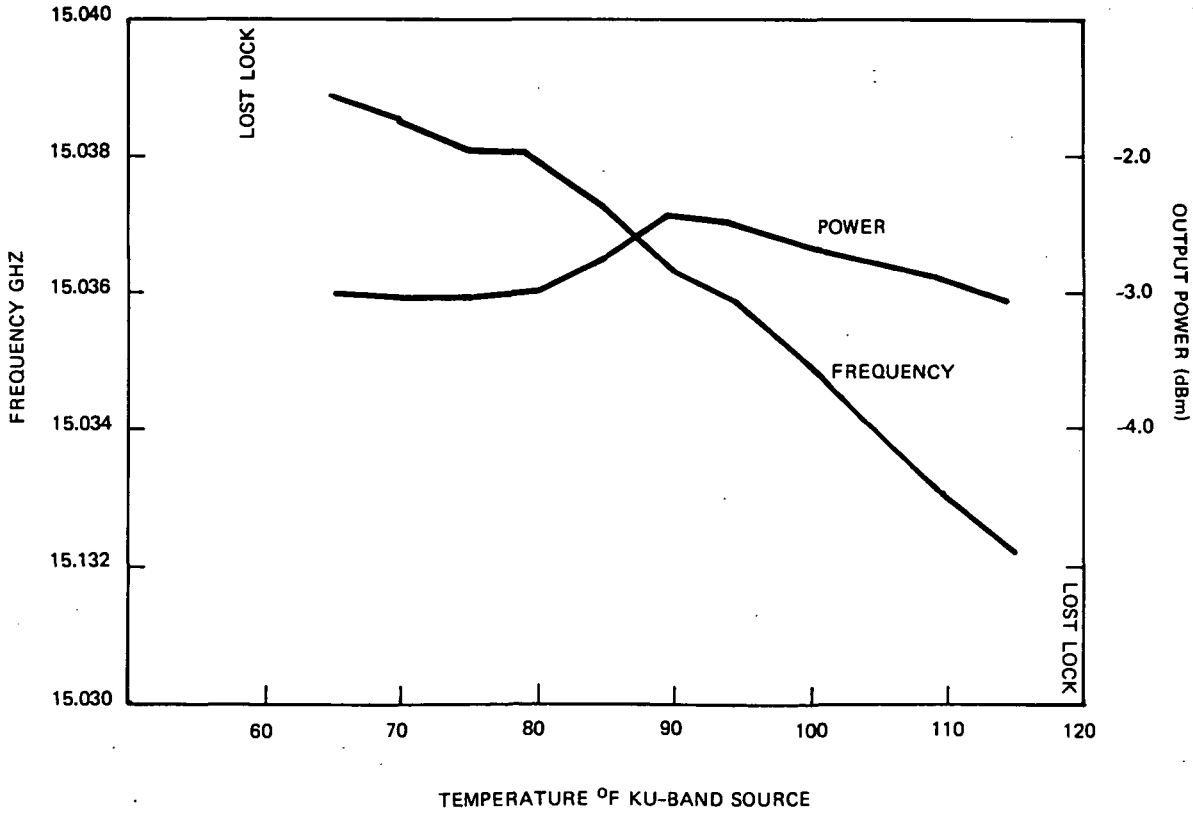

Figure 5-18. Ku-Band Source Temperature Data

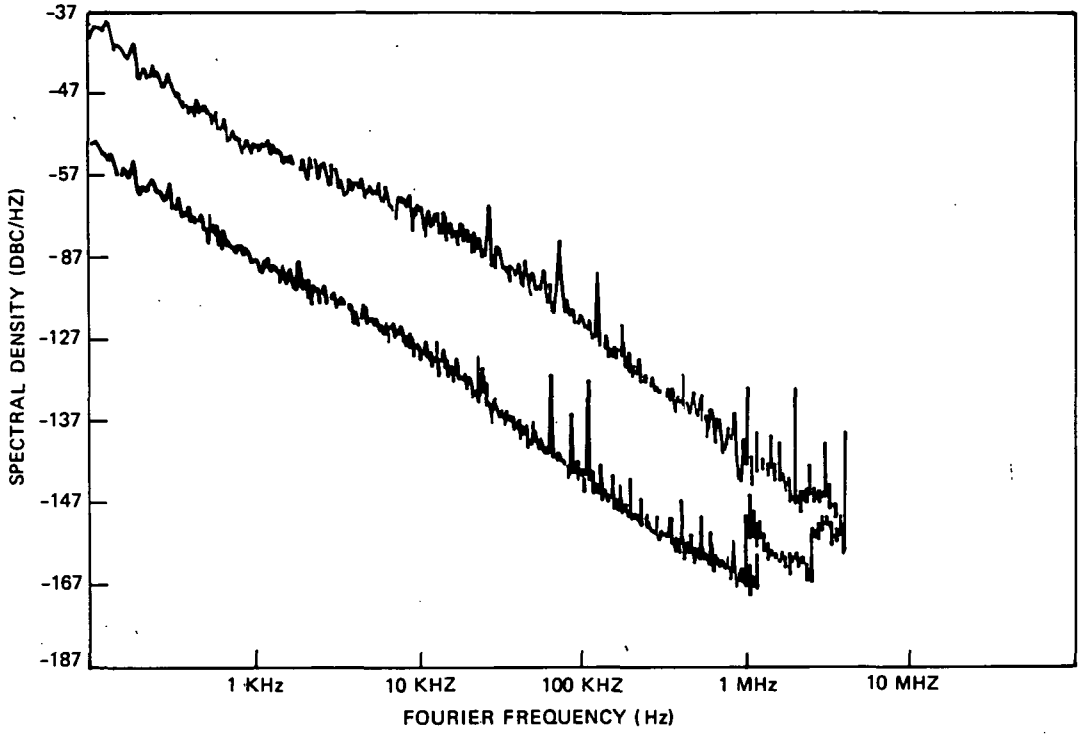

Figure 5-19. Multiplier Type Source Phase Noise

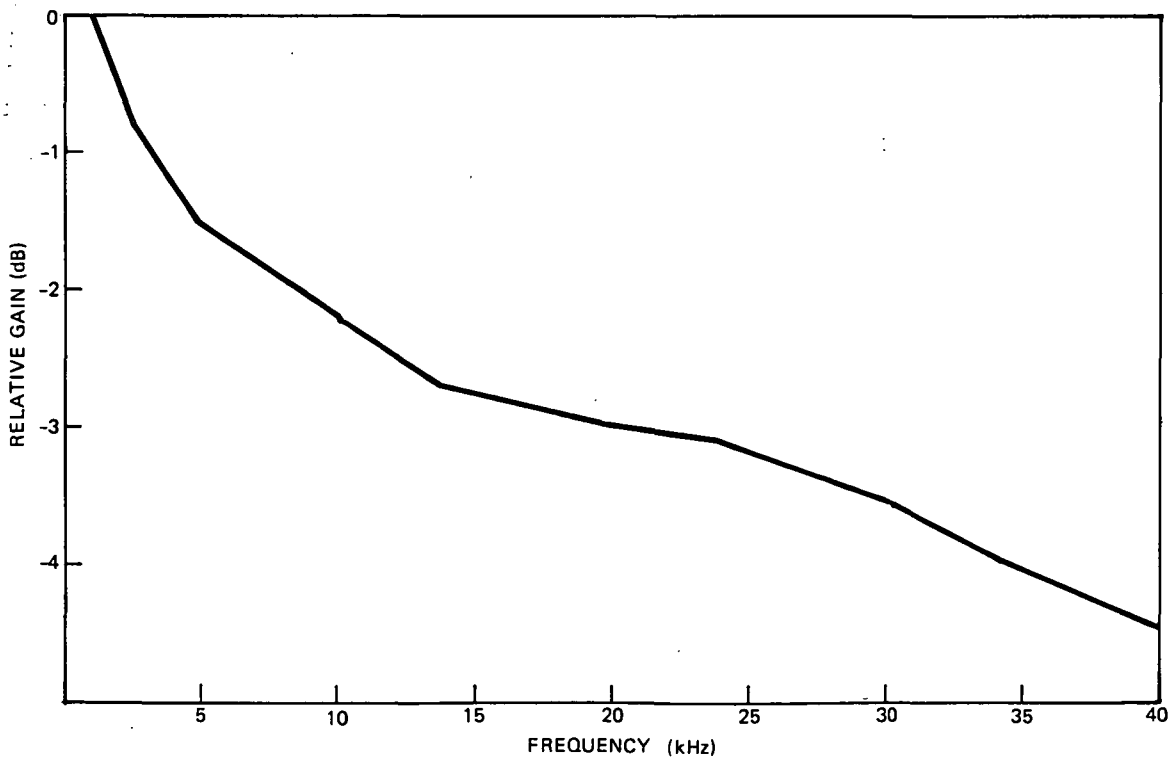

Figure 5-20. Ku-Band Source Loop Bandwidth

5.6 15 GHz DIVIDER SOURCE DESIGN CONCEPT

The 15 GHz divider source was implemented using a combination of hybrid packaged MIC circuits and discrete circuit components assembled on a duroid interconnect board. The 15 GHz source is made up of two assemblies interconnected with coaxial cables (see Figure 5-21). One 3.6 x 8.0 x 0.9 inch assembly contains the 2.14 GHz hybrid packaged SAW oscillator, the 15 GHz hybrid packaged FET VCO, and the hybrid loop amplifier. The second 2.7 x 4.0 x 0.9 inch assembly contains the TED divider and the phase detector circuitry. The complete 15 GHz source is mounted on a 10 x 12 inch aluminum plate.

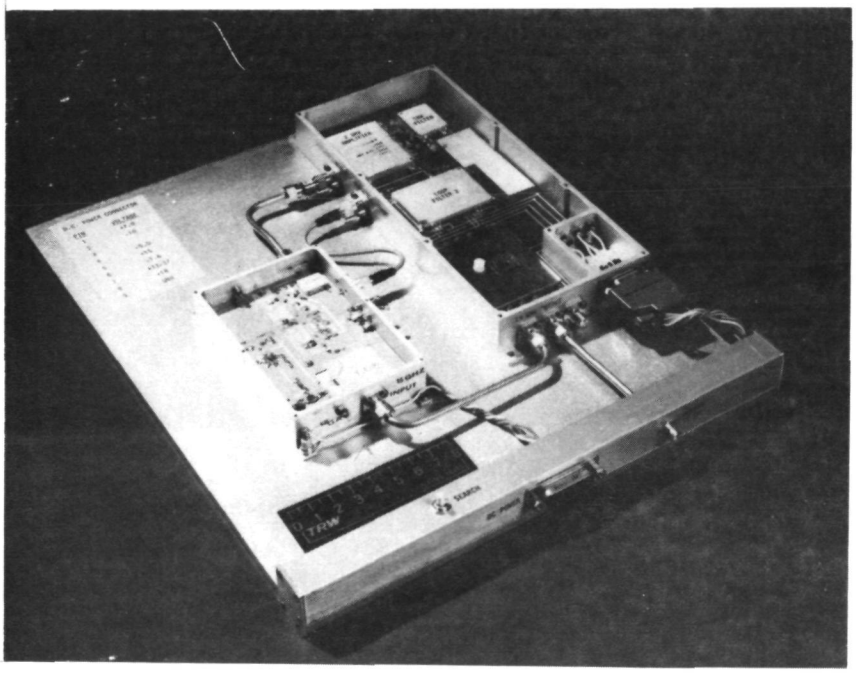

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Figure 5-21. 15 GHz Divider Type Frequency Source

The 2.14 GHz hybrid packaged SAW oscillator, described in Section 3.7 of this report, provides the stable frequency reference to which the 15 GHz FET VCO is phaselocked. The 2.14 GHz output of the SAW oscillator is routed to the second assembly where it is used as the reference for a W-J M4G mixer used as a phase detector.

The output of the M4G phase detector provides the input signal to the loop amplifier hybrid. The loop amplifier hybrid contains the circuitry

necessary to implement a phaselocked loop filter circuit. The loop filter function is realized by building an active lowpass filter using the loop amplifier contained in the loop filter hybrid. All fixed loop filter circuitry is contained in the hybrid; variable parameters are set by external components. In addition to the loop filter function, the loop amplifier hybrid has a sweep acquisition circuit. The sweep acquisition circuit can detect an unlocked loop condition and activate a sweep circuit which will lock the VCO to the reference signal. The output of the loop filter controls the frequency of the FET VCO.

The FET VCO is a 2.5 x 1.7 x 0.3 inch Kovar hybrid package containing four FET amplifier stages with their bias circuits, two 3 dB Lange couplers, a thin varactor tuned cavity resonator, and several sections of adjustable length microstrip transmission line. The oscillator frequency was set at 15 GHz with an output power of 1 dBm at each output port. The oscillator can be tuned over an 11 MHz frequency range electronically with a 1 to 15 volt tuning voltage. The frequency stability of the oscillator is determined by a 0.05 inch thick high Q cavity resonator which has been integrated into the floor of the hybrid package. The output frequency can be adjusted by tuning the cavity. One of the FET VCO outputs is the 15 GHz source output port, the other drives the input of the TED frequency divider.

The TED divider provides a 2.14 GHz output signal which is phase coherent with the 15 GHz input signal from the FET VCO. The TED divider and its temperature compensation circuit are described in detail in Section 4 of this report. The 2.14 GHz TED output is amplified by two Avantek hybrid amplifiers. The amplified 2.14 GHz from the TED drives the feedback input of the M4G phase detector.

5.7 DIVIDER TYPE SOURCE DETAILED DESIGN

A detailed block diagram of the divider type 15 GHz source is shown in Figure 5-22. The divider source is made of six functional circuits, three TRW hybrid circuits, two commercial hybrid circuits, and one discrete component circuit. The TRW hybrid circuits are repackaged versions of the FET VCO, SAW oscillator, and loop amplifier developed earlier in the program. The commercial hybrid circuits are the W-J M4G mixer used as a phase detector and two Avantek UTO series MIC amplifiers used to amplify the 2.14 GHz

output signal from the TED. The discrete component circuit is the TED divider and its temperature compensation circuit. The hybrid circuits and the discrete components are assembled on a duroid circuit board using microstrip transmission line interconnects. The three TRW hybrids, FET VCO, loop amp, and SAW oscillator are housed in one unit. The commercial hybrids and the TED circuitry are housed in the second unit.

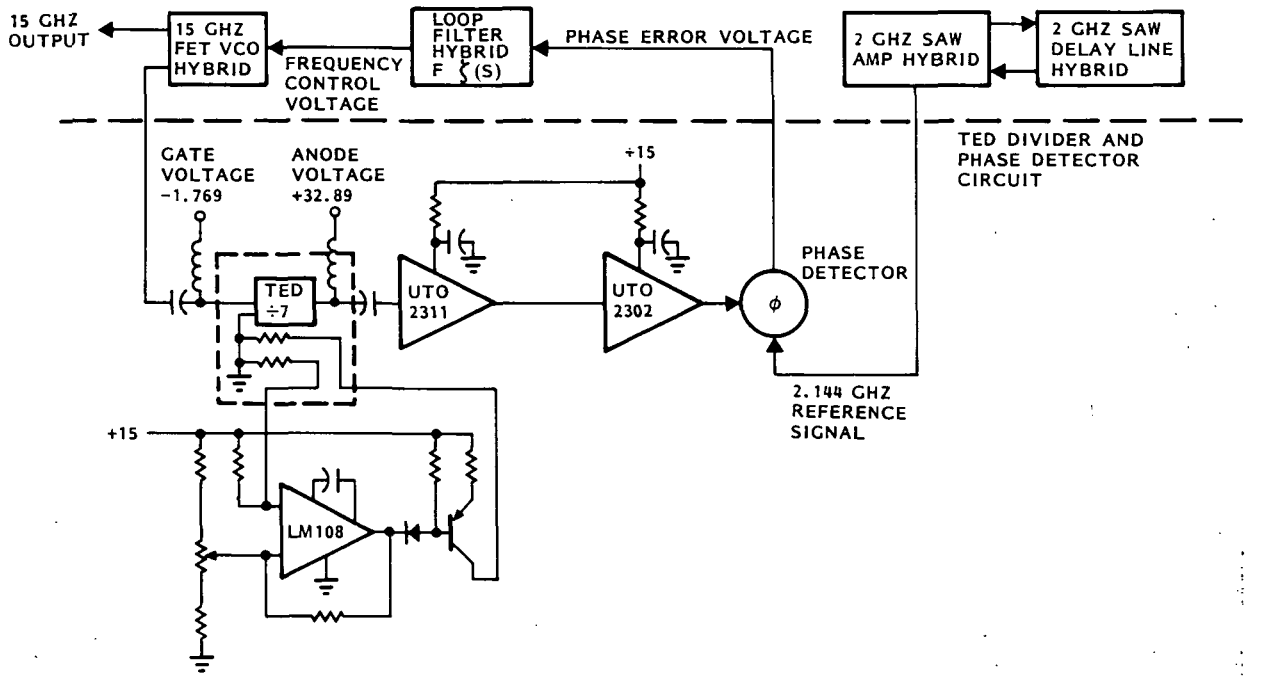

Figure 5-22. Divider Type Source Block Diagram

5.7.1 Hybrid Packaged FET VCO

The 15 GHz FET VCO is a hybrid packaged version of the FET VCO described in Section 6.3 of this report. The hybrid packaged FET VCO was designed so it could be flight qualified; i.e., the mechanical design and assembly techniques are flight compatible and qualified equivalent parts are available. Figure 5-23 is a block diagram of oscillator configuration used in the hybrid FET VCO.

The FET VCO is assembled in a 2.5 x 1.7 x 0.3 inch Kovar package. The package is a custom design fabricated at TRW. RF and dc interfaces with the FET VCO are made via 50 ohm hermetic glass feedthrough terminals which have been brazed into the package walls at nine locations. The package has

RF grounding ears located on either side of the RF interconnect terminals. The 15 GHz cavity resonator is machined directly into the floor of the hybrid package. The cavity is coupled to the RF circuit via pins which enter the cavity through holes in the package's internal floor. The bottom of the cavity is formed by a brazed-in plug which is flush with the bottom of the package. Figures 5-24, 5-25, and 5-26 describe the package configuration and the cavity assembly detail.

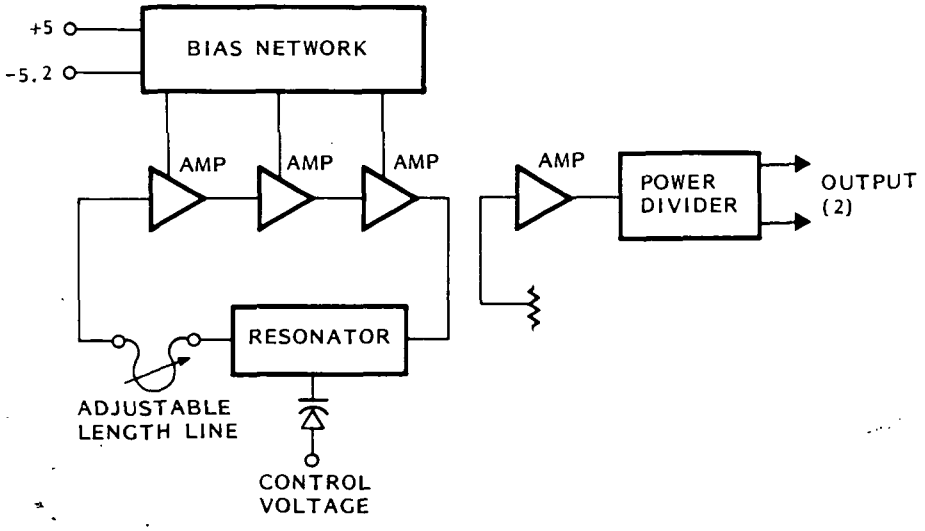

Figure 5-23. FET Oscillator Block Diagram

The FET VCO circuitry is contained on eight interconnect alumina substrates. The eight FET VCO substrates are:

- DC bias substrate
- FET amp input substrate
- Two FET amp interstage substrates
- FET amp interstage/power splitter substrate
- FET amp output/power divider substrate
- Cavity interconnect substrate
- Interconnect line substrate.

A detailed schematic diagram, Figure 5-27, shows the circuitry contained on each substrate.

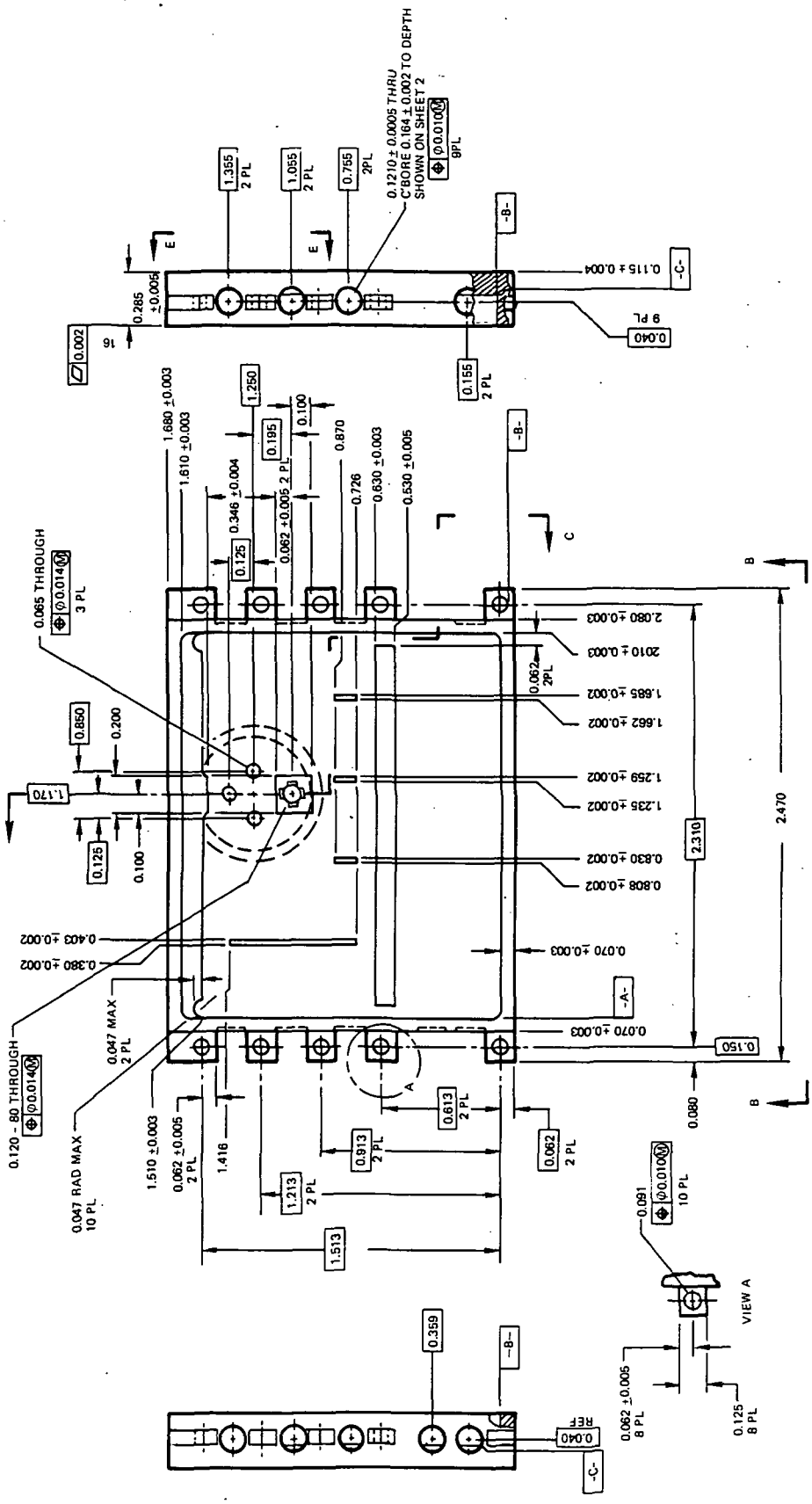

Figure 5-24. FET VCO Package Drawing

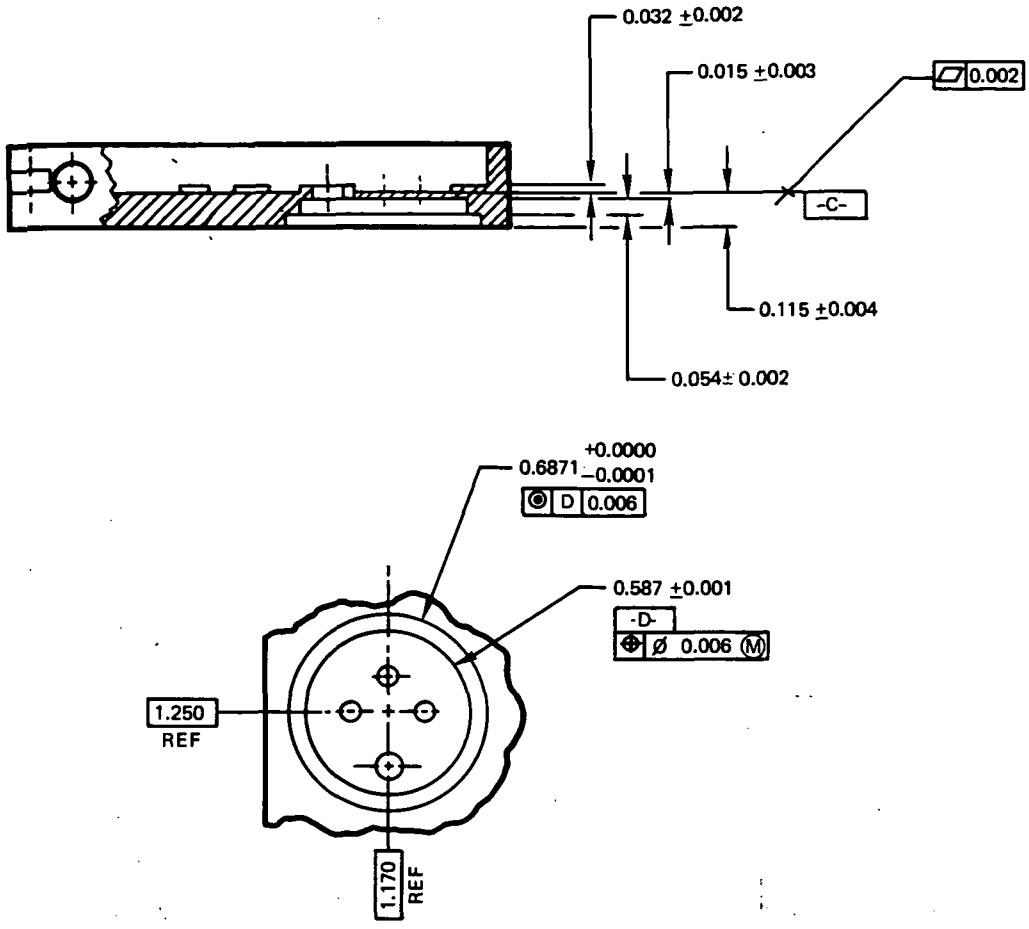

Figure 5-25. Cavity Resonator Detail

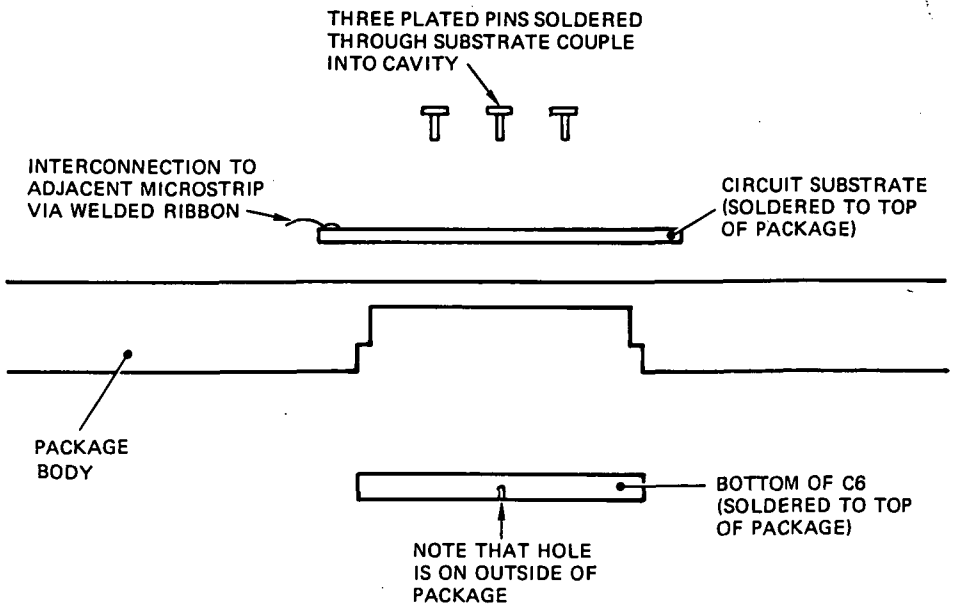

Figure 5-26. Exploded View-Cavity Assembly

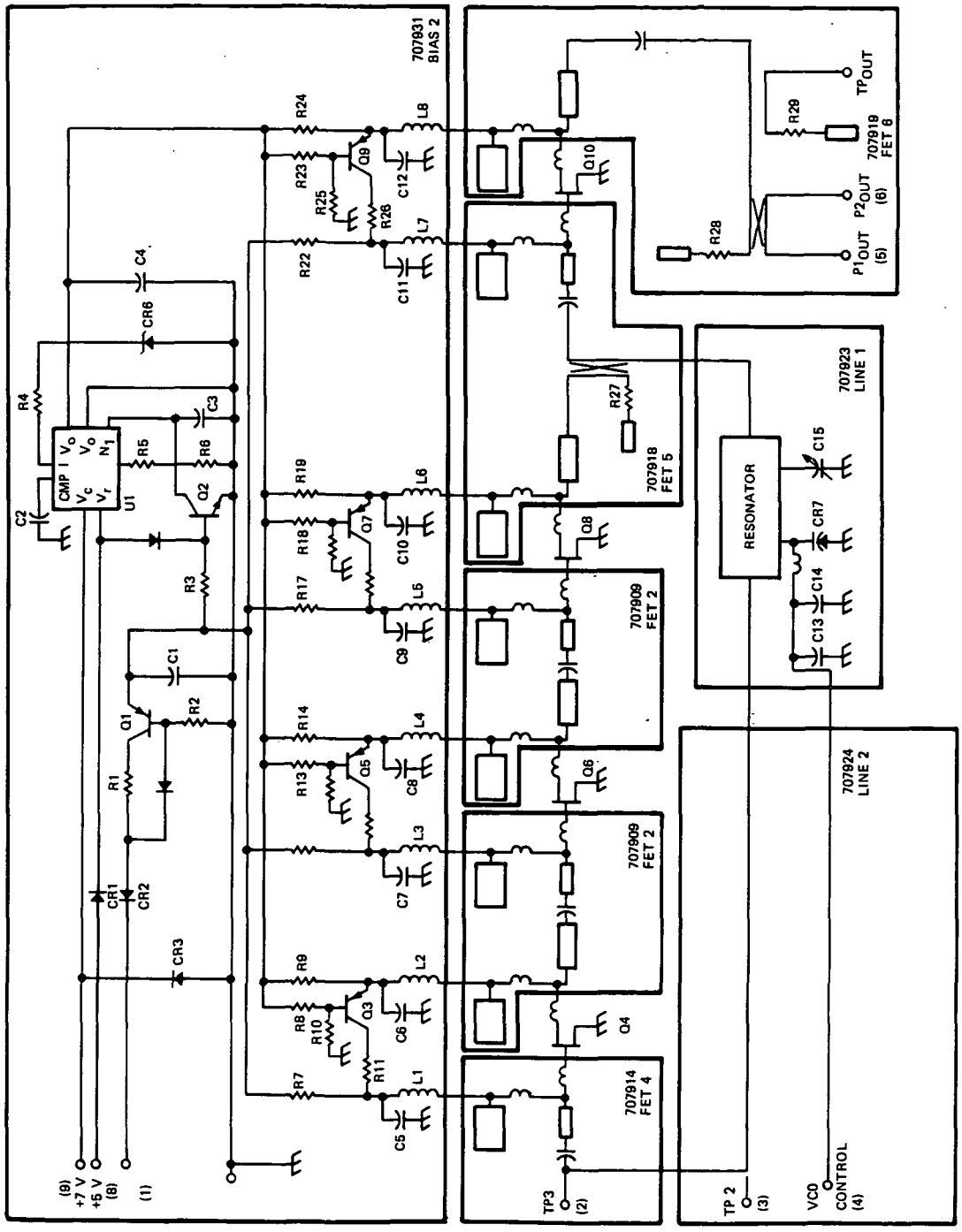

Figure 5-27. FET VCO Schematic Diagram

The FET VCO amplifiers are built with the NE388 devices using microstrip RF matching elements fabricated on an alumina substrate. The FET's are mounted on a ridge which has been machined into the floor of the hybrid package.

The FET amplifier RF circuitry is on the substrates which are eutectically attached to the hybrid package floor between the FET mounting ridges. The connection between the FET and its RF circuitry is made with 0.0007 inch diameter gold wire. The dc bias is applied to the FET's via RF decoupling networks consisting of an inductor made of a length of 0.005 inch diameter gold wire which passes through a narrow slot in a 0.1 inch thick ferrite wall separating the RF and bias sections of this circuit.

The bias circuit, which is the largest substrate in the hybrid, contains the active bias circuitry for the four FET amplifier stages. The bias circuit also contains a voltage regulator circuit and protective circuitry which prevents circuit damage if improper supply voltages are applied.

Figure 5-28 is a photo of the interior of the hybrid packaged 15 GHz FET VCO with each of the substrates and key components identified. A complete parts list of the hybrid is included as Figure 5-29.

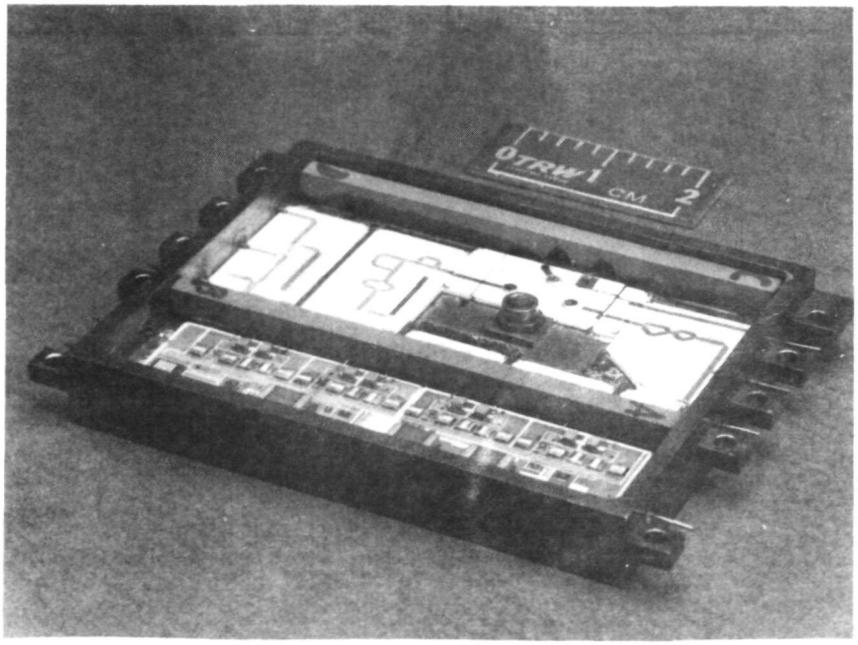

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Figure 5-28. Ku-Band FET VCO

PART NO.	NAME	TYPE	POWER DISSIPATION (MW)	CURRENT (MA)
U1	IC	LM723 (1 TO 52)	180	
Q1	TRANSISTOR	2N2907A (1 TO 21)	6	
Q2	TRANSISTOR	2N2222A (1 TO 18)	1	
Q3, 5, 7, 9	TRANSISTOR	2N2907A (1 TO 21)	1	
Q4, 6, 8, 10	FET	NE38800	60	
CR1	DIODE	1N3604 (1 TO 20)	4	3
CR2	DIODE	1N3604 (1 TO 20)	1.5	1.5
CR3	DIODE	1N5811 (1 TO 46)	0	0
CR4	DIODE	1N5297 (1 TO 46)	4	1
CR5	DIODE	1N5297 (1 TO 46)	17	1
CR6	DIODE, ZENER	1N753A (1 TO 19-011Z)	0	0
CR7	VARACTOR	GC1600A (1 TO 60)	0	0
R1	RESISTOR	DEPOSITED, 1K ±20%	2.5	1.5
R2	RESISTOR	DEPOSITED, 6.2K ±5%	6.2	1.0
R3	RESISTOR	DEPOSITED, 3K ±5%	3.0	1.0
R4	RESISTOR	DEPOSITED, 3K ±5%	8.3	1.7
R5	RESISTOR	DEPOSITED, 4.3K ±5%*	1.0	0.5
R6	RESISTOR	DEPOSITED, 10K ±5%*	2.5	0.5
R7, 12, 17, 22	RESISTOR	33K ± 10% (1K055)	1.1	0.3
R8, 13, 18, 23	RESISTOR	3.6K ± 5%* (1K055)	1.6	0.7
R9, 14, 19,24	RESISTOR	180 ± 5% (1K055)	18	10
R10, 15, 20, 25	RESISTOR	3.9K ± 5%* (1K055)	1.7	0.7
R11, 16, 21, 26	RESISTOR	4.7K ± 10% (1K055)	0.5	0.3
R27, 28, 29	RESISTOR	DEPOSITED, RF TERMINATION	N/A	N/A
L1, 2, 3, 4, 5, 6, 7, 8	INDUCTOR	0.005 GOLD WIRE SUBSTRATE INTERCONNECT		
C1, 3, 4	CAPACITOR	BX. CHIP, 0.1 μF ±20% (1A074)		
C2	CAPACITOR	BX. CHIP, 1000 pf ±20% (1A074)		
C5, 6, 7, 8, 9, 10, 11, 12	CAPACITOR	NPO CHIP, 100 pf ±10% (1A074)		
C13	CAPACITOR	NPO CHIP, 33 pf ±10% (1A074)		
C14	CAPACITOR	DICAP, 3.6 pf ±0.1 pf (1A079)		
C15	TUNER	JOHANSON 6924-3, THREAD 0.120 X 80 MOUNT (8P017)		

*NOMINAL TOLERANCE SHOWN HERE, BUT THESE RESISTORS HAVE TIGHTER MATCHING TOLERANCE.

Figure 5-29. FET VCO Parts List

The results of the final tests on the FET VCO are summarized in Table 5-4. Figure 5-30 is a plot of the phase noise characteristics and the hybrid FET VCO. The temperature tests indicated that improvements in the cavity temperature coefficient and the phase shift range of the varactor phase shifter would be necessary for operation over the full temperature range. This can be accomplished by using an Invar cavity resonator and upgrading the phase shifter design.

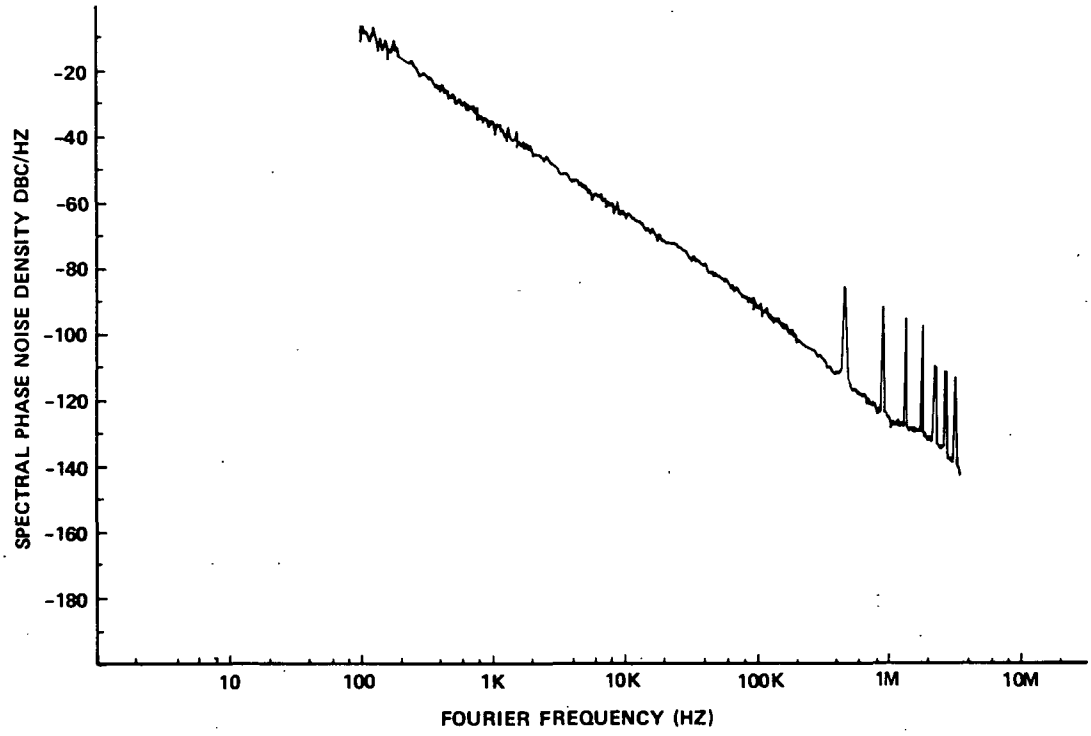

Figure 5-30. Hybrid FET Oscillator Phase Noise

5.7.2 Loop Amplifier

The loop amplifier hybrid contains the loop error signal conditioning and loop control circuitry. The operation and basic circuit of the loop amplifier hybrid is identical to that of the loop filter circuit described in Section 6.3 of this report. The only significant circuit change is that the components determining loop filter characteristics have not been included in the hybrid. By controlling the loop filter characteristics with components external to the hybrid, the circuit can be easily tailored to operate with a specific FET VCO and phase detector. This feature also

Table 5-4. FET VCO Performance Summary

Specification	Design Goal	Performance
Frequency	15.00 GHz	15.0 GHz
Tuning Range	±8 MHz	±5.5 MHz
Output Power		
Ports 1 and 2	+4.5 dBm ±0.75 dB	+1.0 dBm
Test Point	>-10 dBm	>-10 dBm
Tuning Voltage	2 to 13 volts	2 to 13 volts
Tuning Sensitivity	1.6 MHz/volt	1.0 MHz/volt
Tuning Input Impedance	>1 KΩ, <100 pf	>1 KΩ, <100 pf
Phase Noise		
1 kHz	-50 dBc/Hz	-36 dBc/Hz
10 kHz	-80	-64 dBc/Hz
100 kHz	-100	-92 dBc/Hz
1 MHz	-120	-126 dBc/Hz
150 MHz	-140	-126 dBc/Hz
DC Power	+15 volts at 3 mA	+15 volts at
	+7 volts at 60 mA	7 volts at
	-10 volts at 1 mA	-10 volts at
	Total expected power, 450 mW	
Temperature Range		
Breadboard	0^{o} to 120^{o}F	
Size	1.65 x 2.15, 7 pin package	1.7 x 2.5, 9 pin package
Stability	Unconditional, any load VSWR	Unconditional

allows the loop amplifier hybrid to be used as the loop filter in other phaselocked loop applications. The schematic diagram of the hybrid loop amplifier is shown in Figure 5-31. The loop filters external components are shown on the schematic diagram connected to the hybrid's interface points with dashed lines. The loop filter can be tailored to form a low-pass characteristic anywhere in the <1 to >10 kHz range. The loop amplifier output voltage is 2 to 13 volts with a source impedance of less than 500 ohms. The loop amplifier requires 315 mW from a 15 volt supply and 78 mW from a -5.2 volt supply. The hybrid operates over a -10 to +50°C temperature range. The loop amplifier hybrid is a 12 lead 1.295 x 0.72 inch butterfly type package. Details of the loop amplifiers construction can be seen in Figure 5-32.

5.7.3 TED Divider and Phase Detector Module

The TED divider and phase detector module contains the temperature-compensated TED divider circuit (see Section 4.9) and the 2 GHz phase detector circuit. A block diagram of the module is shown in the lower portion of Figure 5-21. The TED divider is mounted on an alumina subassembly which has been integrated with the duroid module interconnect board. The low level 2.14 GHz output signal from the TED divider is amplified by two Avantek amplifiers, a UTO-2311 and a UTO-2302. The +10 dBm output signal of the UTO-2302 drives the signal input of the W-J M4G mixer used as a phase detector. The output and the reference input of the phase detector are connected to the loop filter and the SAW oscillator which are housed in the other Ku-band source module. The TED divider and phase detector module circuitry was assembled on a duroid interconnect board which is mounted in a machined aluminum housing. The complete TED divider and phase detector module is shown in Figure 5-33.

5.8 DIVIDER SOURCE DATA SUMMARY

The performance of the complete Ku-band divider type frequency source is shown in Table 5-5. The Ku-band divider type source consists of the hybrid 15 GHz FET VCO which has been phaselocked to a 2.14 GHz SAW oscillator using a TED divide-by-seven circuit.

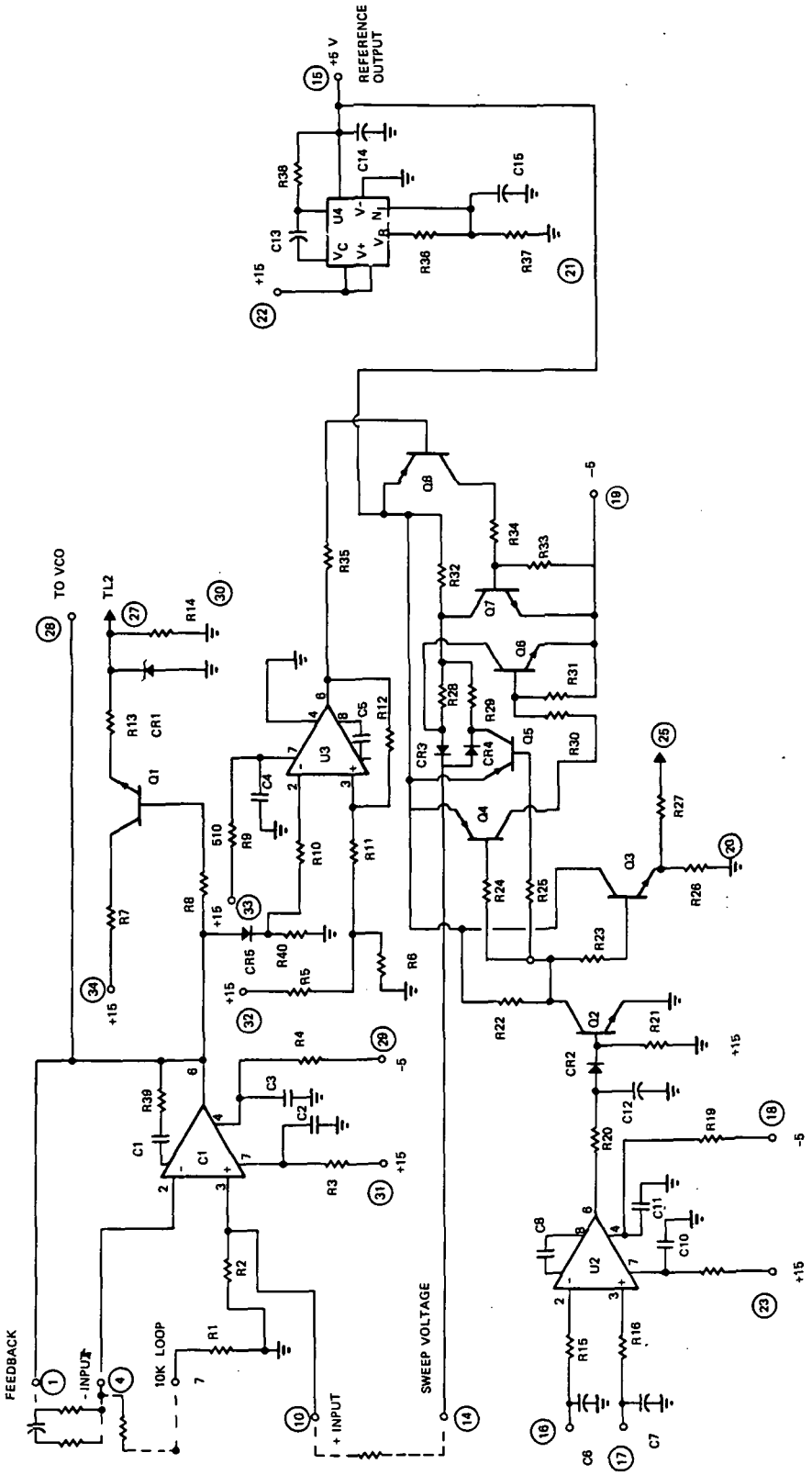

Figure 5-31. Loop Filter Schematic Diagram

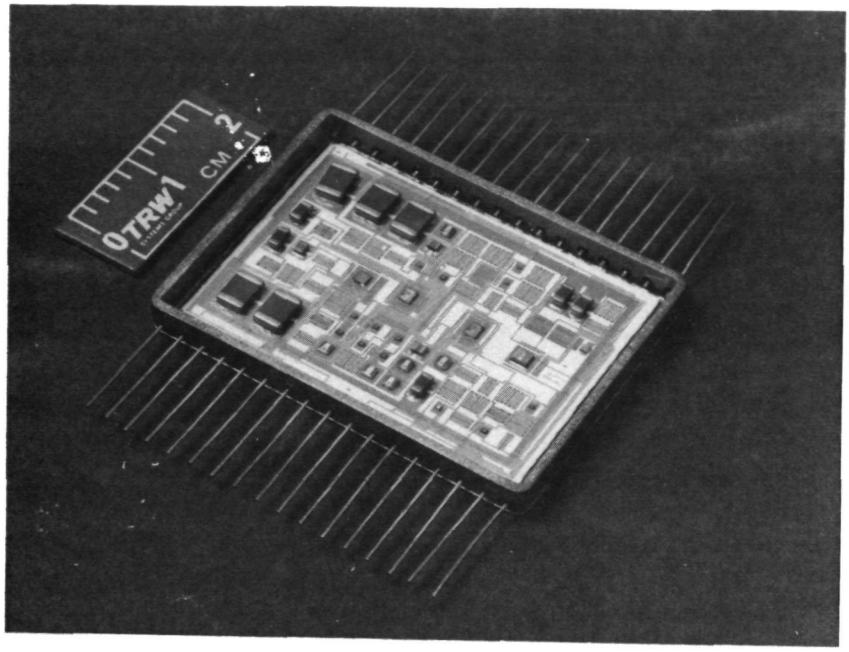

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Figure 5-32. Loop Amplifier II

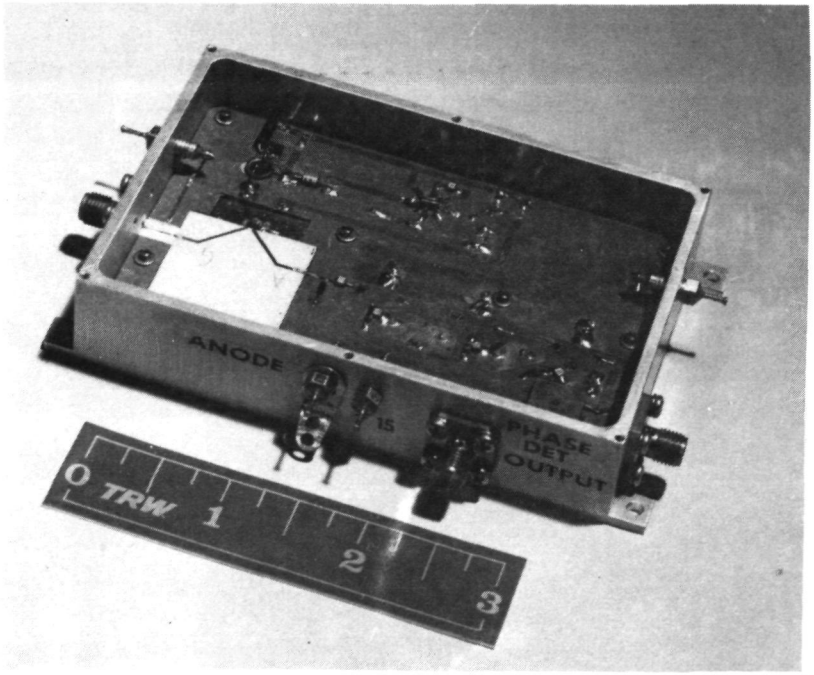

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Figure 5-33. TED Divider Assembly

Table 5-5. Ku-Band Divider Type Frequency Source Performance Summary

Parameter	Performance
Frequency	15.001 GHz
Temperature Stability	±0.029 percent (±4.35 MHz)
Phase Noise	
100	-30 dBc/Hz
1 kHz	-18 dBc/Hz
10 kHz	-66 dBc/Hz
100 kHz	-92 dBc/Hz
1 MHz	-126 dBc/Hz
Output Power	-1.5 dBm ±0.25 dB
DC Power	3.9 watts
Temperature Range	10^{o}C to 37^{o}C
Spurious (10 to 18 GHz)	-60 dBc

The temperature stability, aging, and close-in phase noise are directly related to the SAW oscillator. The phase noise characteristics outside the phaselocked loop bandwidth are a function of the 15 GHz FET VCO. Figure 5-34 is a plot of the complete Ku-band source's phase noise characteristic. The phase noise was measured over a frequency range from 100 Hz to 3 MHz away from the source output frequency.

The divider type source operated over a temperature range of 50 to 98^{o}F, considerably less than the desired 0 to 120^{o}F temperature range. The reduced temperature range is due to the limited temperature operating range of the FET VCO.

The temperature shift of the FET VCO is greater than the FET VCO's control range. When the frequency shifts outside the VCO control range, the phaselocked loop circuit loses control of the VCO and the source breaks lock.

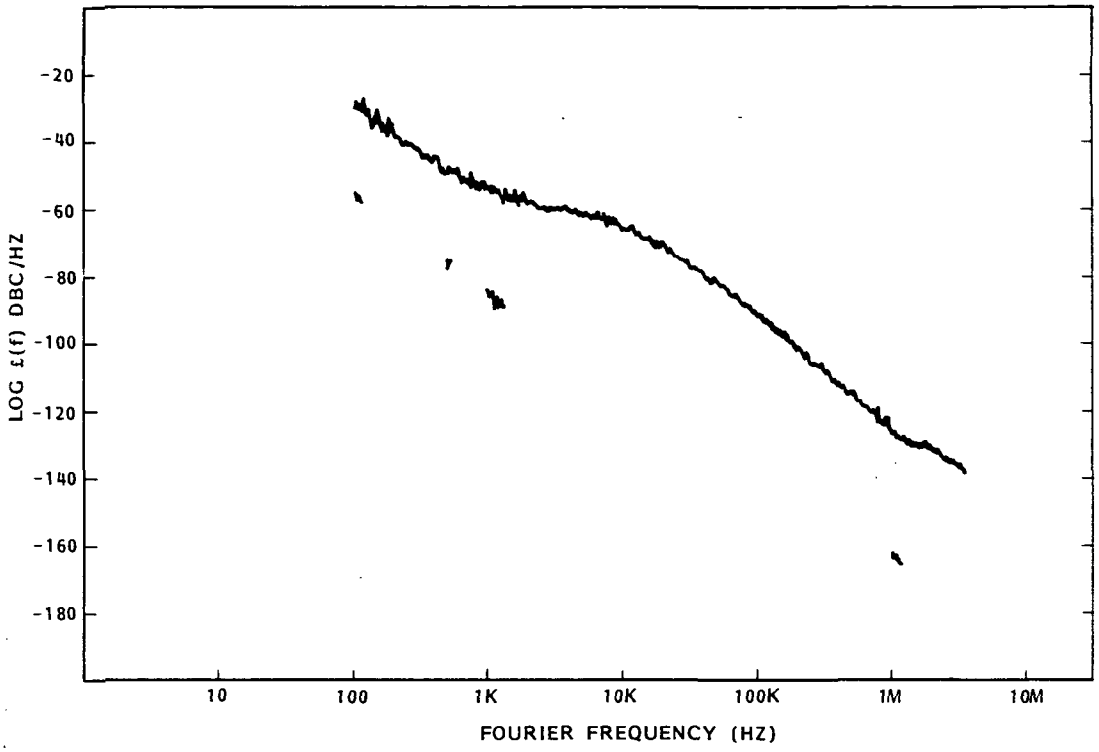

Figure 5-34. Ku-Band Source Phase Noise

5.9 15 GHz SOURCE PERFORMANCE COMPARISON

A comparison of the two Ku-band sources is shown in Table 5-6. In general, the performance of the two sources is very similar. The phase noise characteristics, however, exhibit an interesting phenomenon (see Figure 5-35). The phase noise of the divider source is better than the multiplier source in the 100 Hz to 1 kHz range, although its 2.14 reference is 10 dB noisier. The high noise level inside the loop bandwidth indicates that a loop component in the multiplier source is responsible for a noise level approximately 14 dB higher than in the divider source. Two possible noise sources are the phase detector and the loop filter circuit. The loop filter circuits are nearly identical, which leaves the phase detectors as the likely source of the excess noise. The phase detector used in the multiplier type source is a quadrature type circuit operating at 15 GHz. The 15 GHz phase detector has an output level of 4 mV/deg. The divider type phase detector is a Watkins-Johnson M4G mixer operated at 2 GHz. The 2 GHz phase detector has an output level of 17 mV/deg. This difference in signal

level at the low signal point of the phaselocked loop circuit represents a change of 13 dB in signal-to-noise ratio and explains the degraded loop performance. The phase noise of the divider source is approximately 5 dB greater than the multiplier source outside the loop bandwidth, at frequencies greater than 10 kHz from the carrier.

Table 5-6. Ku-Band Frequency Source Performance Summary

Parameter	Performance	
	Hybrid Version	Discrete Version*
Frequency	15.001 GHz	15.035 GHz
Temperature Stability	+0.029 percent (±4.35 MHz)	+0.023 percent (±3.36 MHz)
Phase Noise		
100	-30 dBc/Hz	-24 dBc/Hz
1 kHz	-48 dBc/Hz	-53 dBc/Hz
10 kHz	-66 dBc/Hz	-69 dBc/Hz
100 kHz	-92 dBc/Hz	-96 dBc/Hz
1 MHz	-126 dBc/Hz	-132 dBc/Hz
Output Power	-1.5 dBm ±0.25 dB	-2.5 dBm ±0.5 dB
DC Power	3.9 watts	6.1 watts
Temperature Range	10 to 37°C	65°F to 118°F
Spurious (10 to 18 GHz)	<-60 dBc	<-60 dBc

*Developed on NASA contract NAS 5-23822.

The phase noise outside the phaselocked loops bandwidth is due to the FET VCO characteristics. The slightly higher phase noise indicates that the hybrid packaged FET oscillator is noisier than the discrete FET oscillator. The degraded phase performance is not inherent in the hybrid type oscillator, but is caused by increased circuit losses and degraded cavity resonator Q due to assembly problems experienced in fabricating the breadboard hybrid circuit. The assembly problems will be corrected when additional hybrid oscillators are fabricated.

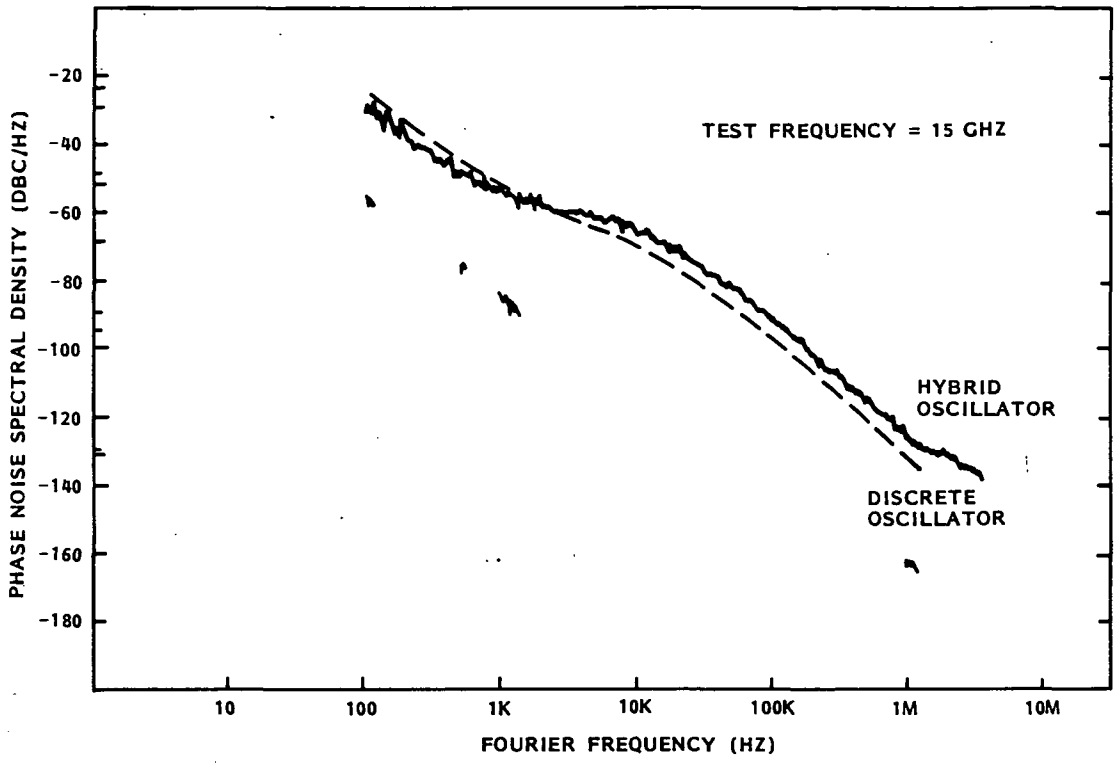

Figure 5-35. Ku-Band Phase Noise Comparison